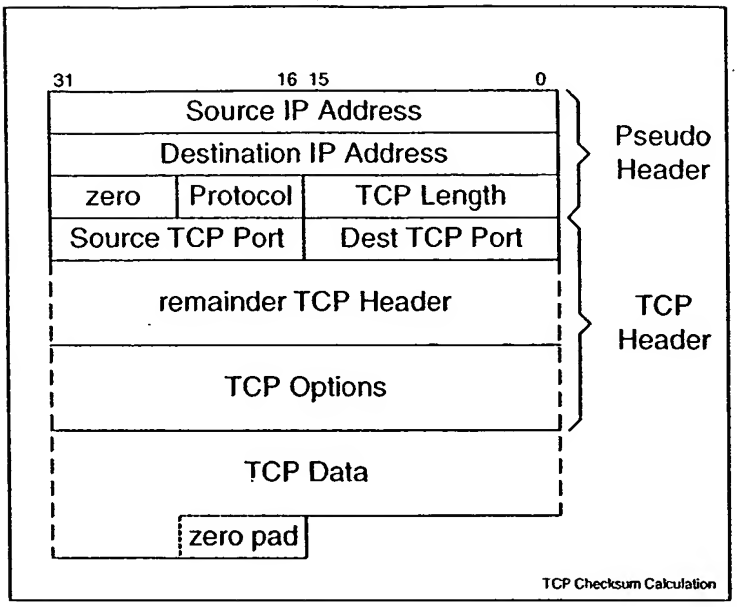

Figure 1A (PRIOR ART)

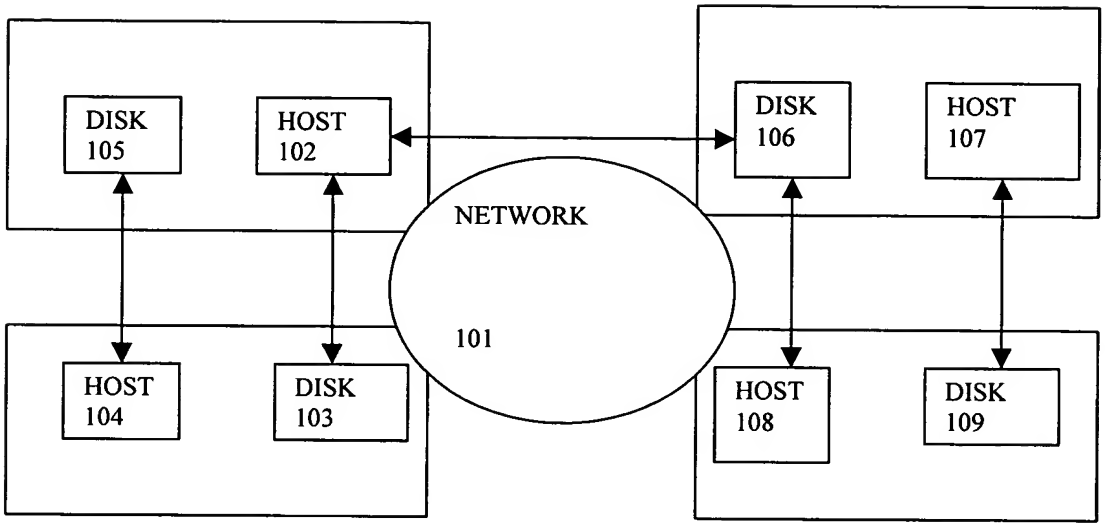

FIGURE 2A

100

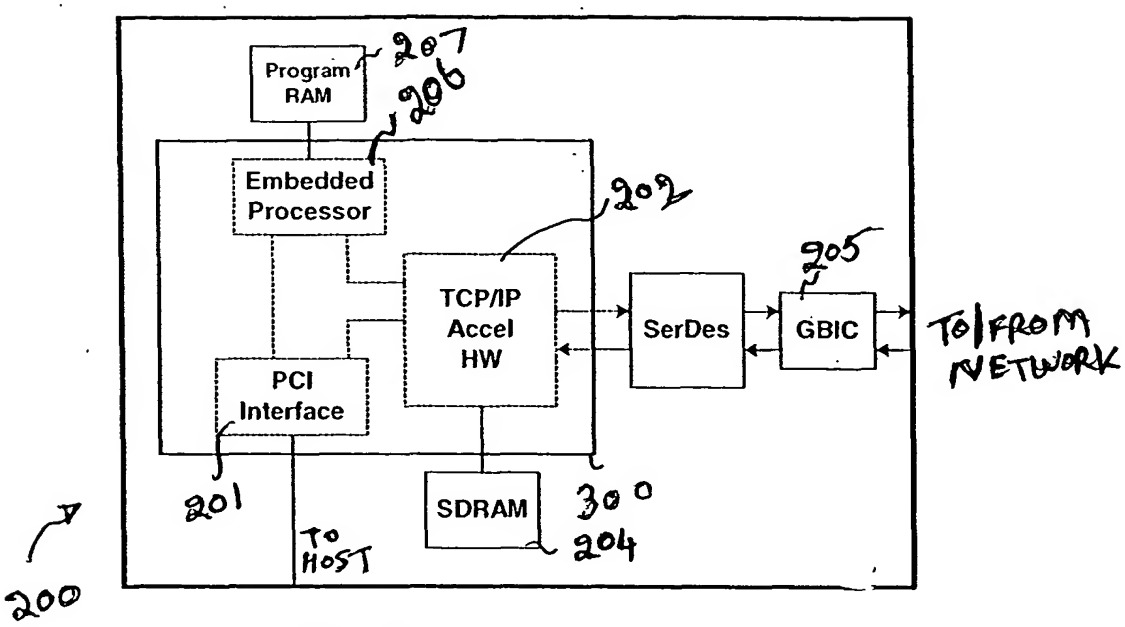

Figure 2B

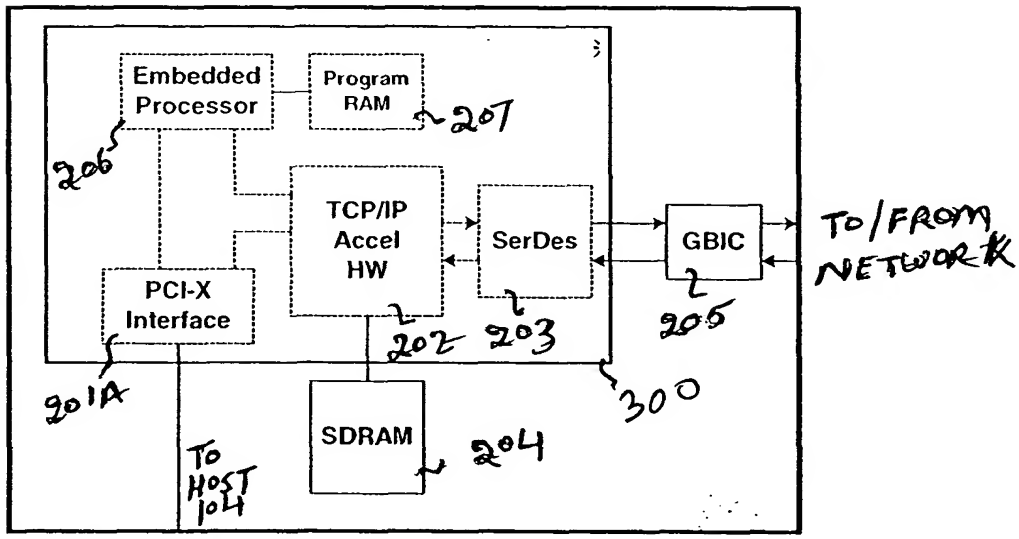

Figure 2C

200A

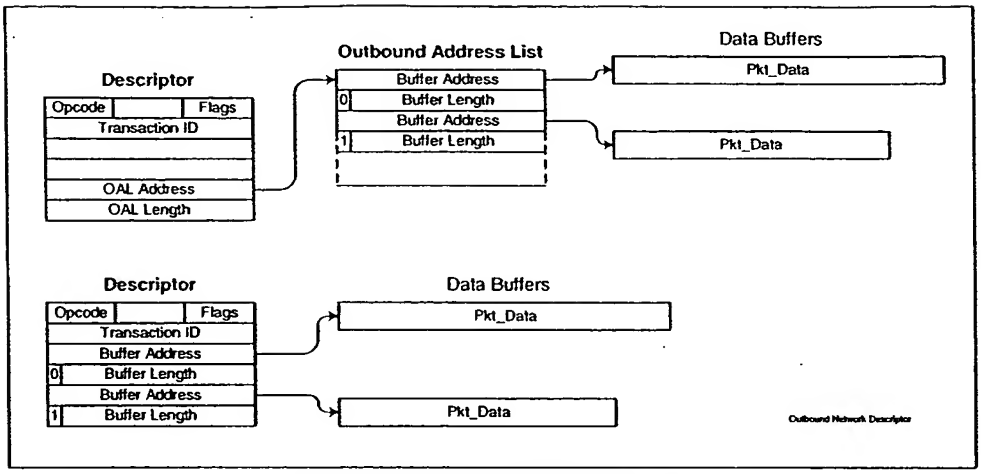

Figure 3A-1 Network IOCB Example

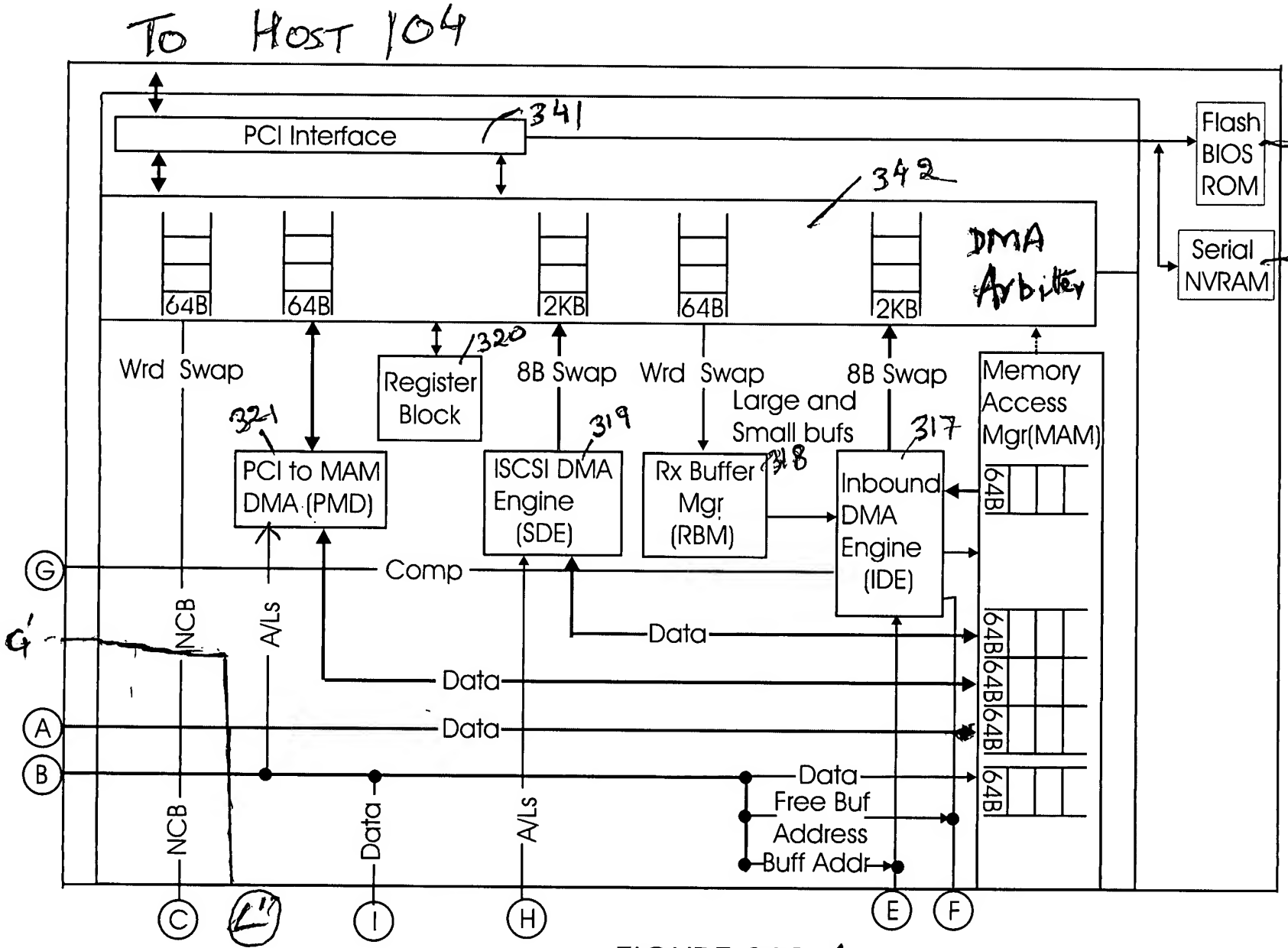
To Host 104
PCI Interface
341
342
Flash BIOS ROM
340
Serial NVRAM
339
DMA Arbiter
64B
64B
2KB
64B
2KB
Wrd Swap
Register Block
320
8B Swap
Wrd Swap
8B Swap
Large and Small bufs
Memory Access Mgr(MAM)
321
319
317
318
PCI to MAM DMA (PMD)
ISCSI DMA Engine (SDE)
Rx Buffer Mgr (RBM)
Inbound DMA Engine (IDE)
64B
G
Comp
G'
NCB
A/Ls
Data
Data
A
Data
B
Data
Free Buf
Address
Buff Addr
64B
64B
64B
64B
NCB
Data
A/Ls
C
I
H
E
F

FIGURE 3A1-1

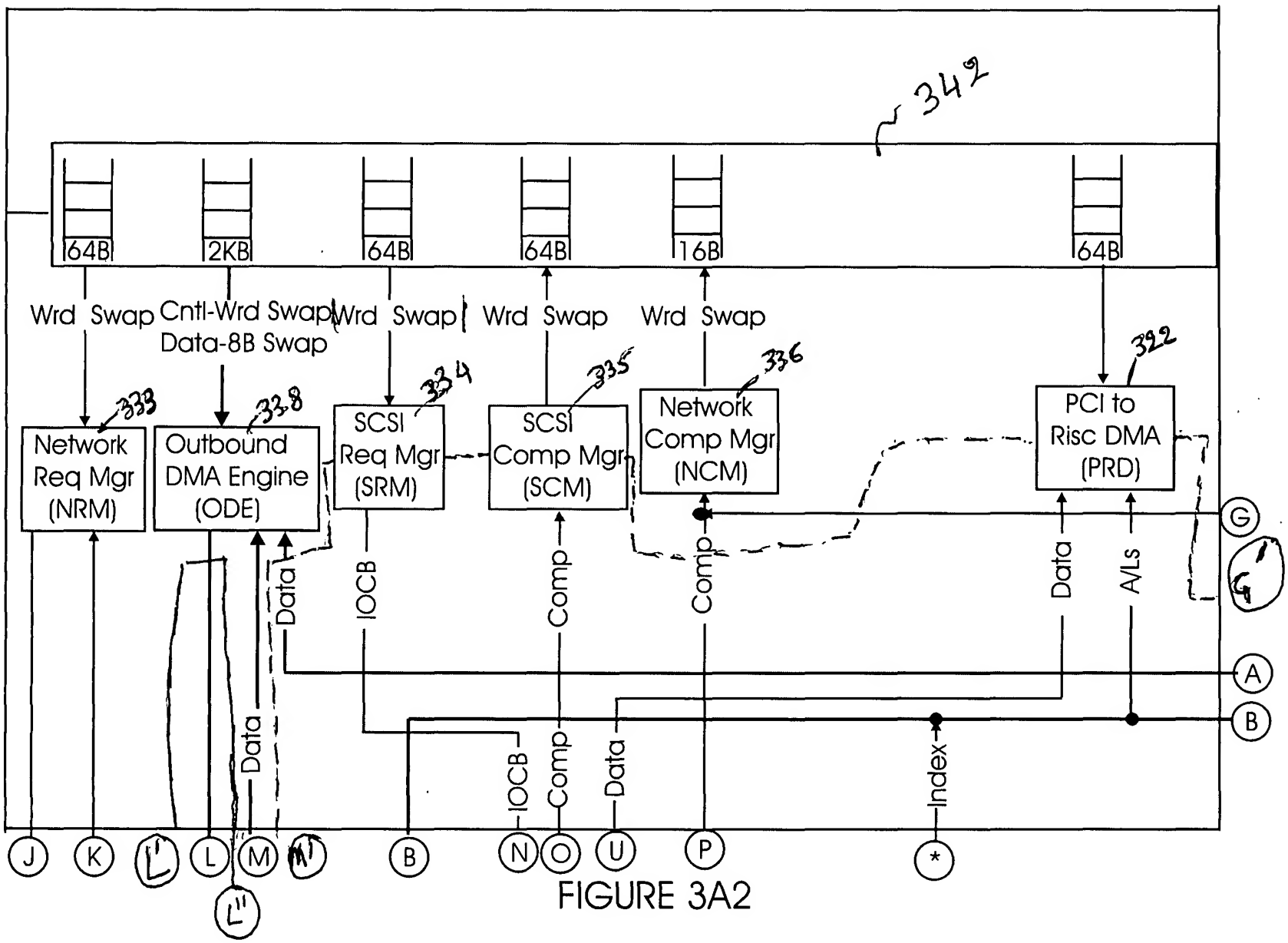
342
64B
2KB
64B
64B
16B
64B
Wrd Swap
Cntl-Wrd Swap
Data-8B Swap
Wrd Swap
Wrd Swap
Wrd Swap
333
338
334
335
336
392
Network Req Mgr (NRM)
Outbound DMA Engine (ODE)
SCSI Req Mgr (SRM)
SCSI Comp Mgr (SCM)
Network Comp Mgr (NCM)
PCI to Risc DMA (PRD)
Data
IOCB
Comp
Comp
Data
A/Ls
G
G'
A
B
Data
IOCB
Comp
Data
Index
J
K
L'
L
M
M'
B
N
O
U
P
*
L''

FIGURE 3A2

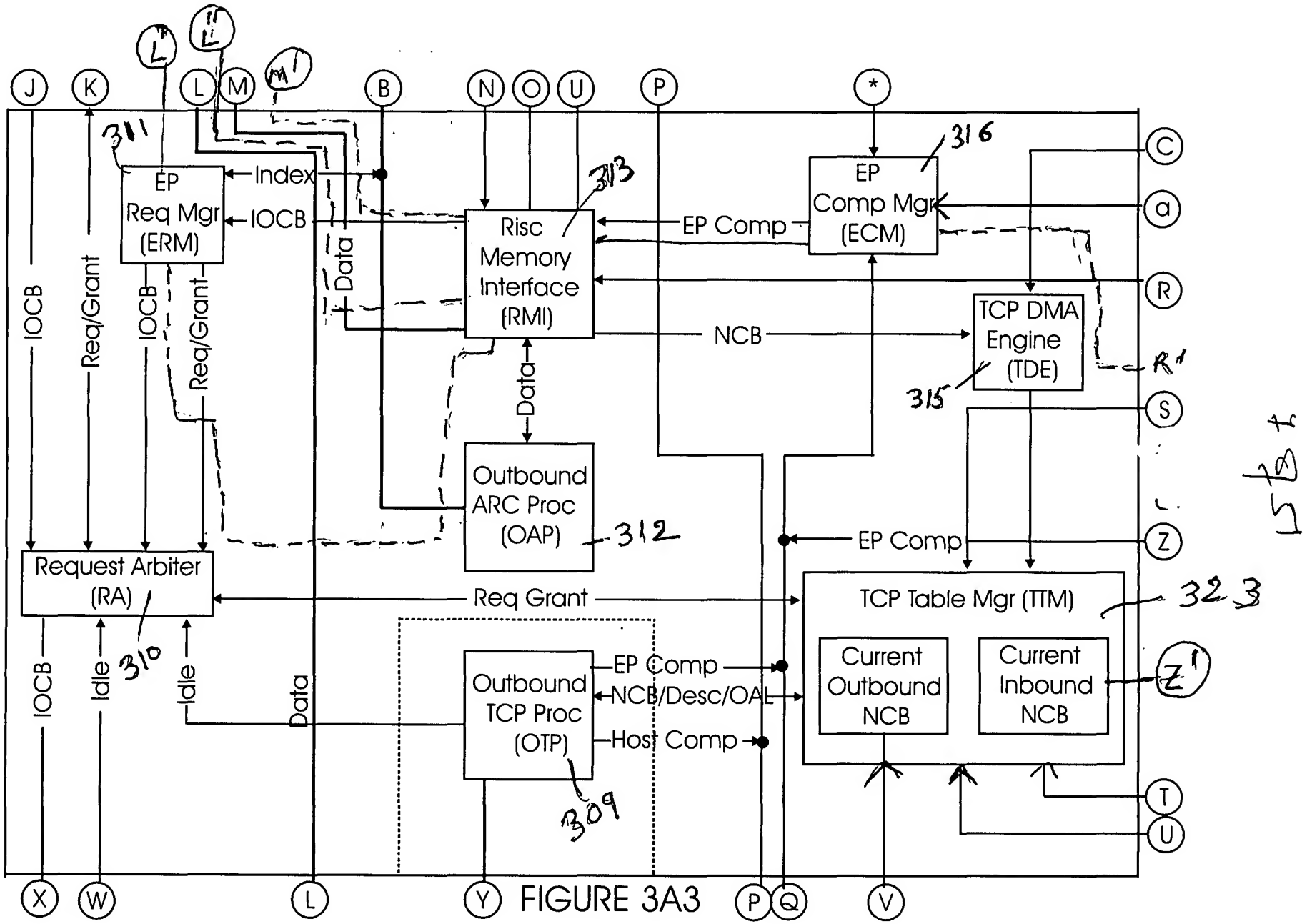
J
K
L
M
B
N
O
U
P
*
C
a
R
S
Z
T
U
X
W
L
Y
P
Q
V
EP Req Mgr (ERM)
Index
IOCB
Data
Risc Memory Interface (RMI)
EP Comp
EP Comp Mgr (ECM)
316
313
311
NCB
TCP DMA Engine (TDE)
315
R'
IOCB
Req/Grant
IOCB
Req/Grant
Data
Outbound ARC Proc (OAP)
312
EP Comp
Request Arbiter (RA)
Req Grant
TCP Table Mgr (TTM)
323
Current Outbound NCB
Current Inbound NCB
Z'
IOCB
Idle
310
Idle
Data
Outbound TCP Proc (OTP)
EP Comp
NCB/Desc/OAL
Host Comp
309

FIGURE 3A3

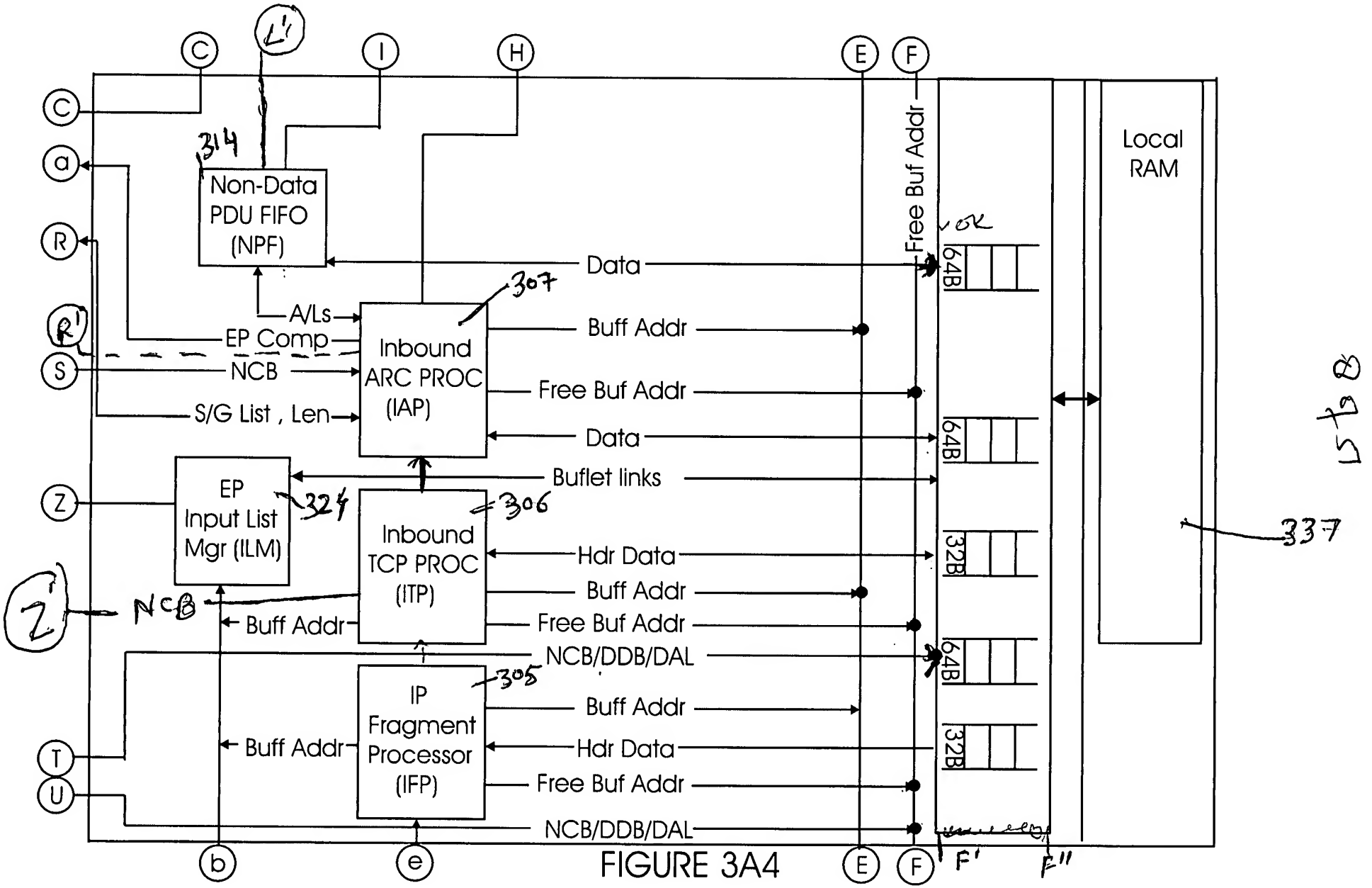
C
L'
I
H
E
F
C
a
R
R'
S
Z
Z'
T
U
b
e
E
F
F'
F''
314
Non-Data PDU FIFO (NPF)
307
Inbound ARC PROC (IAP)
324
EP Input List Mgr (ILM)
306
Inbound TCP PROC (ITP)
305
IP Fragment Processor (IFP)
Data
A/Ls
EP Comp
NCB
S/G List , Len
Buff Addr
Free Buf Addr
Data
Buflet links
Hdr Data
Buff Addr
Free Buf Addr
NCB/DDB/DAL
Buff Addr
Buff Addr
Hdr Data
Free Buf Addr
NCB/DDB/DAL
Free Buf Addr
64B
64B
32B
64B
32B
Local RAM
337

FIGURE 3A4

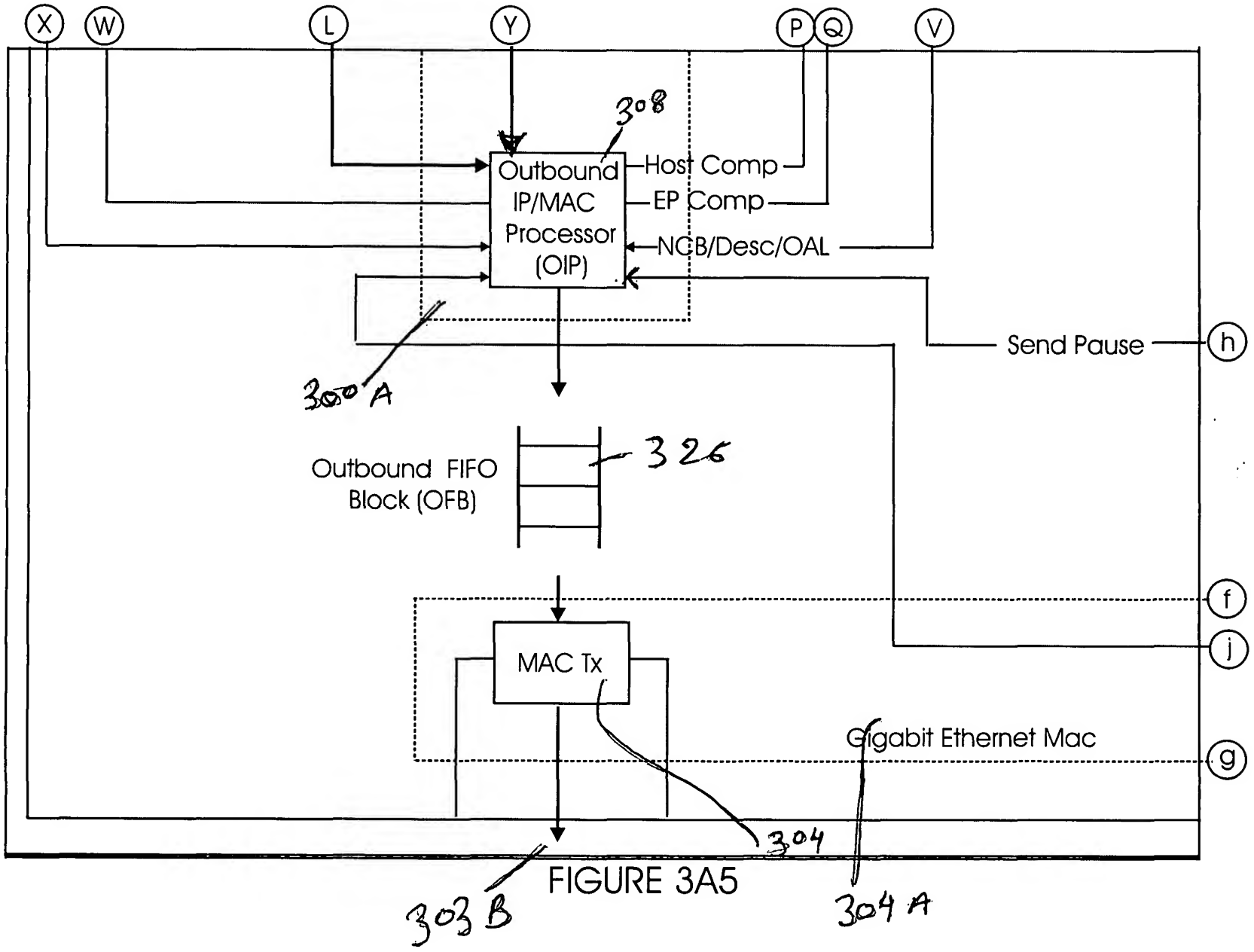
X
W
L
Y
P
Q
V
308
Outbound IP/MAC Processor (OIP)
Host Comp
EP Comp
NCB/Desc/OAL
Send Pause
h
300 A
Outbound FIFO Block (OFB)
326
f
j
MAC Tx
Gigabit Ethernet Mac
g
304
303 B
304 A

FIGURE 3A5

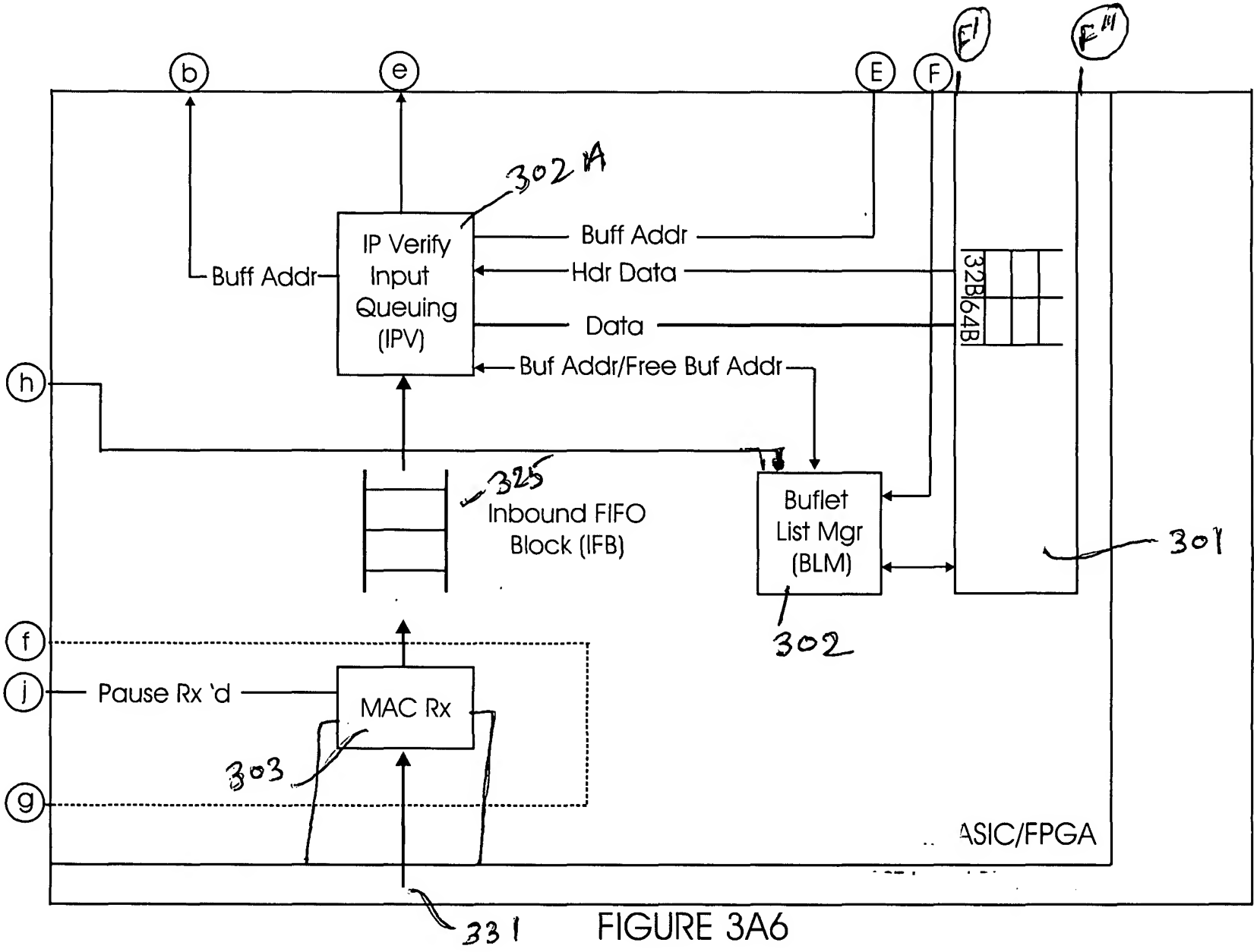
b
e
E
F
E'
F'''
302A
IP Verify
Input
Queuing
(IPV)
Buff Addr
Buff Addr
Hdr Data
Data
Buf Addr/Free Buf Addr
32B
64B
h
325
Inbound FIFO
Block (IFB)
Buflet
List Mgr
(BLM)
301
302
f
j
Pause Rx 'd
MAC Rx
303
g
ASIC/FPGA
331

FIGURE 3A6

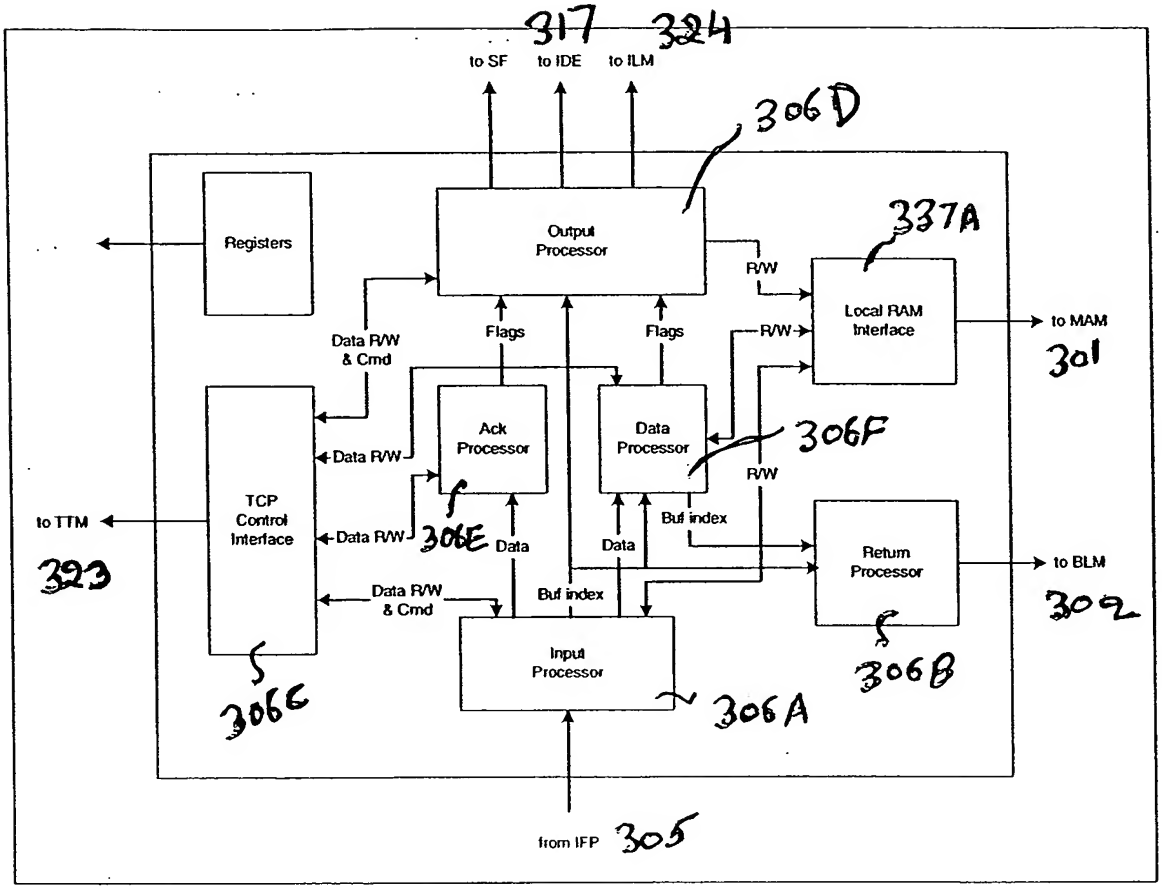
317
324
to SF
to IDE
to ILM
306D
Registers
Output Processor
337A
R/W
Local RAM Interface
to MAM
301
Data R/W & Cmd
Flags
Flags
R/W
Ack Processor
Data Processor
306F
Data R/W
R/W
to TTM
TCP Control Interface
Data R/W
306E
Data
Data
Buf index
Return Processor
to BLM
302
323
Data R/W & Cmd
Buf index
Input Processor
306C
306B
306A
from IFP
305
306

Figure 3B -

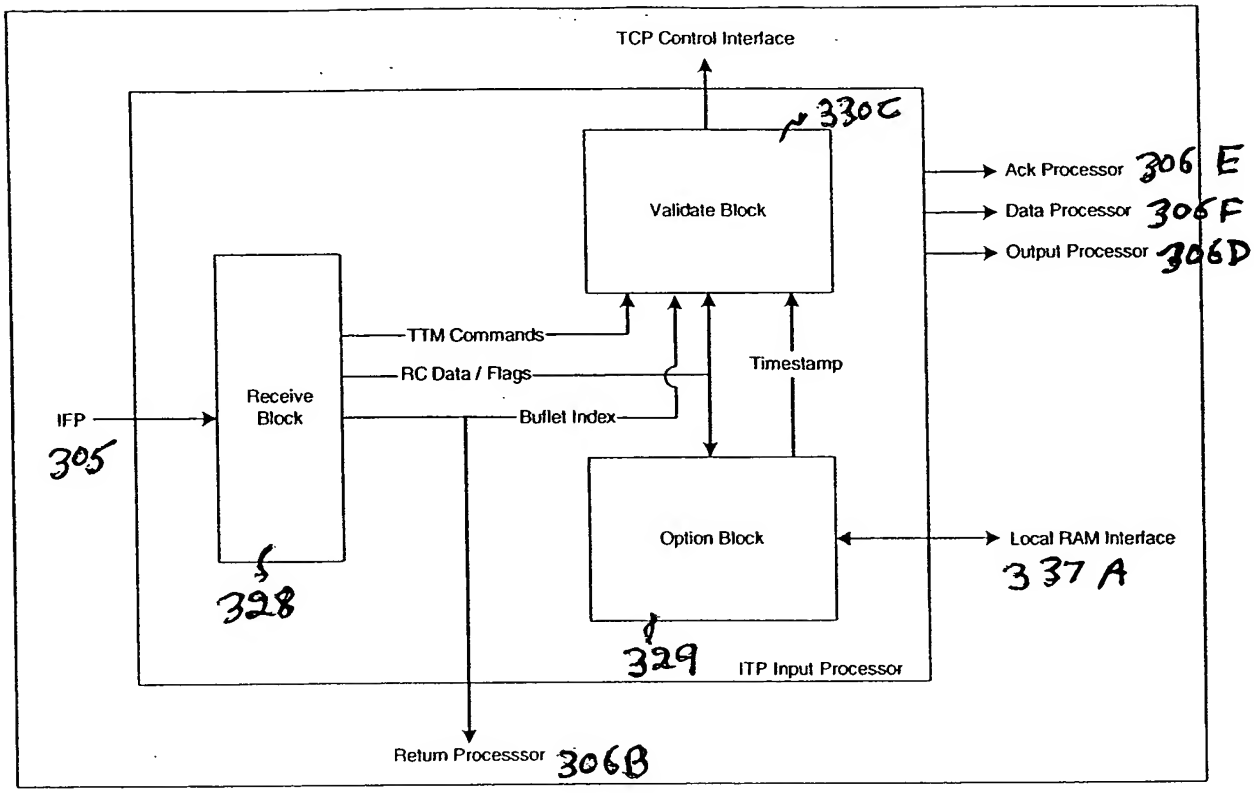

Figure 3C – ITP Input Processor

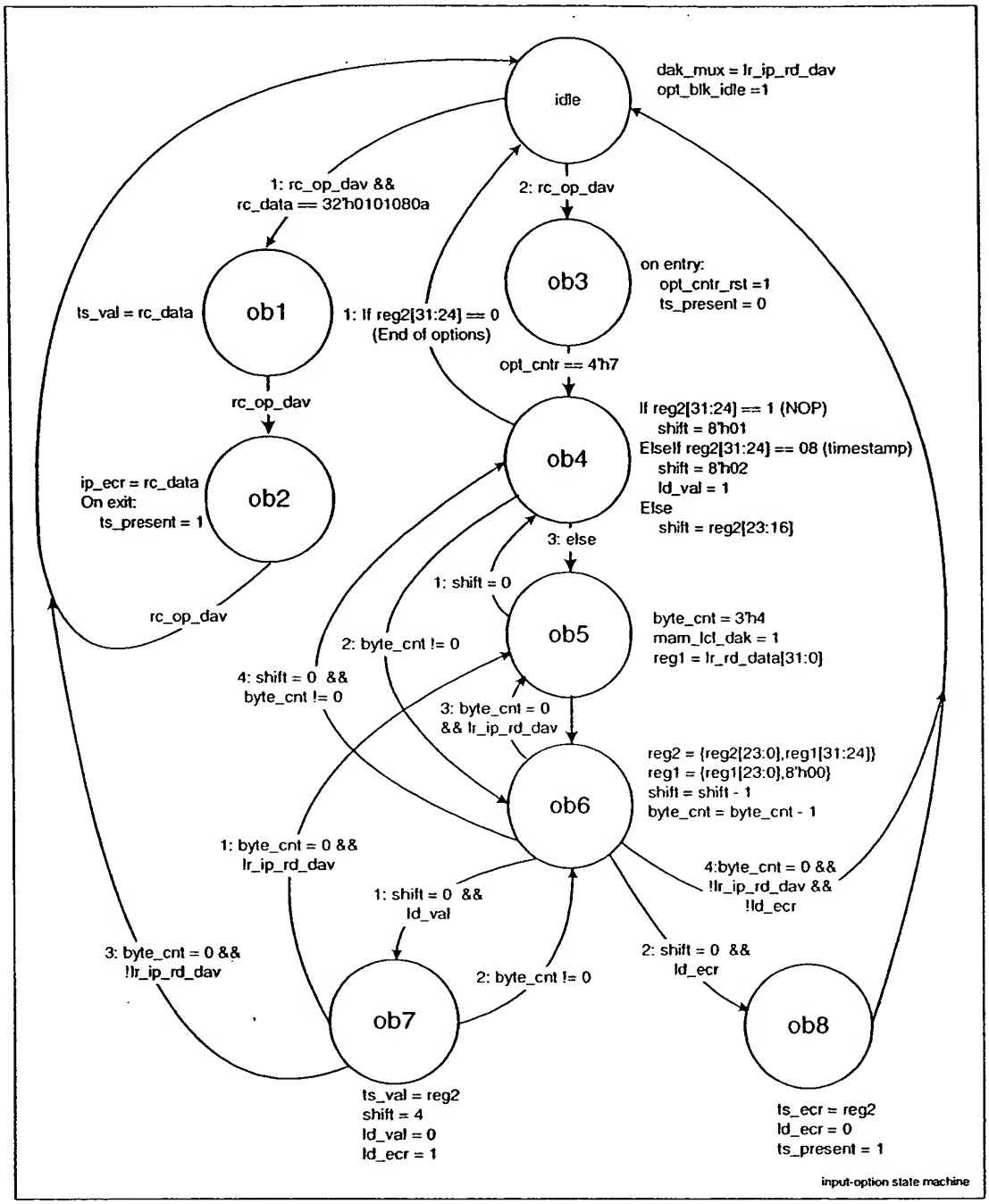

Figure 3C1 Input Processor Option Block State Machine

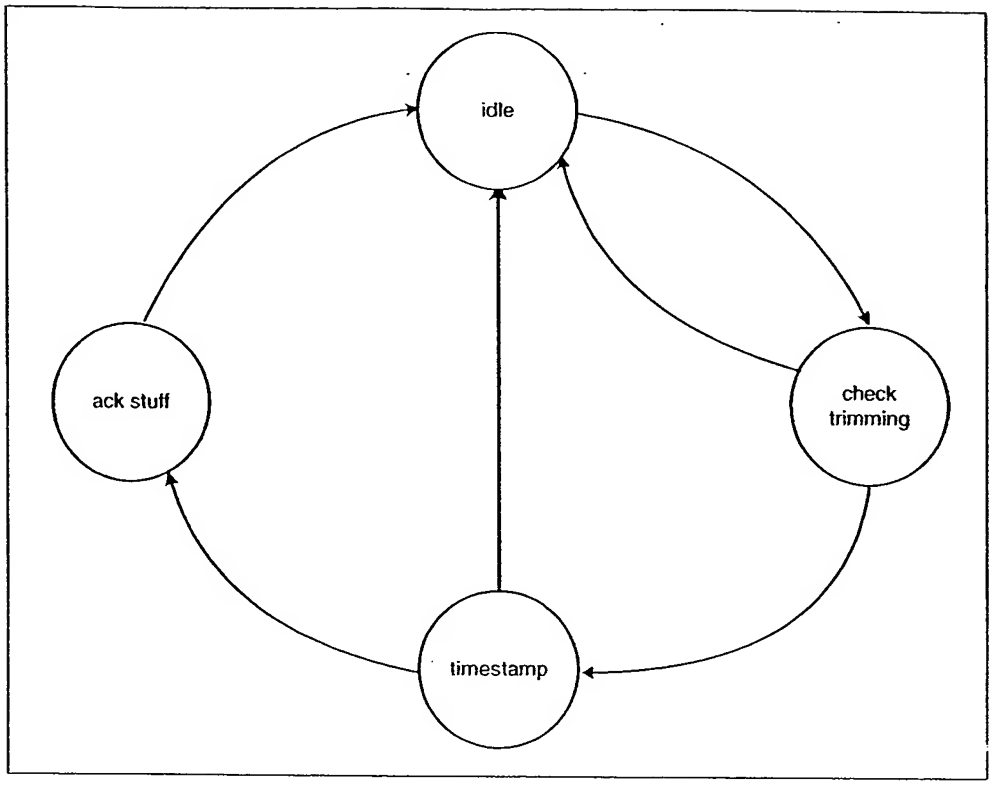

Figure 3C2: Validation State Machine

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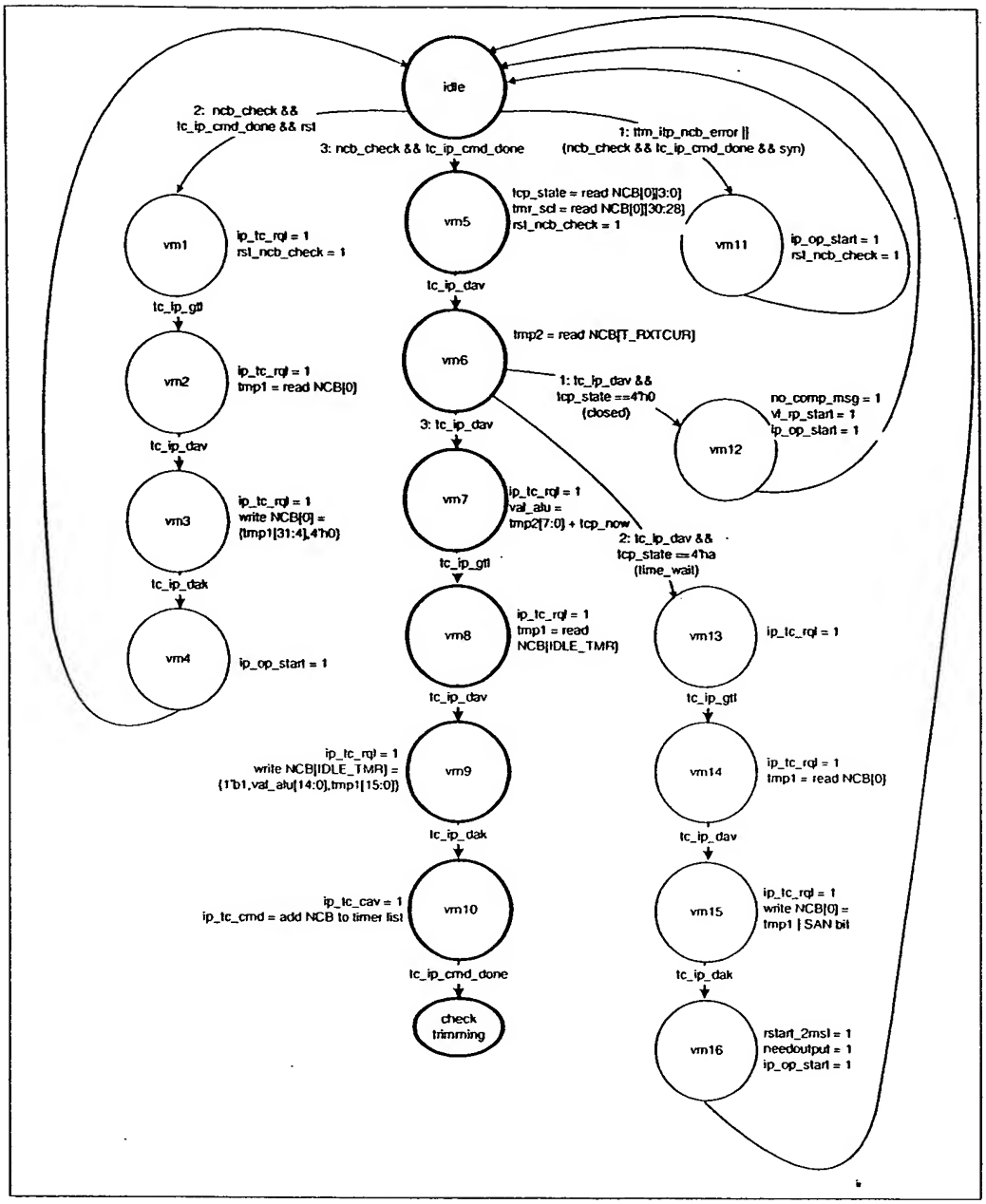

Figure 3C3: Validation State Machine for Reset, SYN or Invalid State

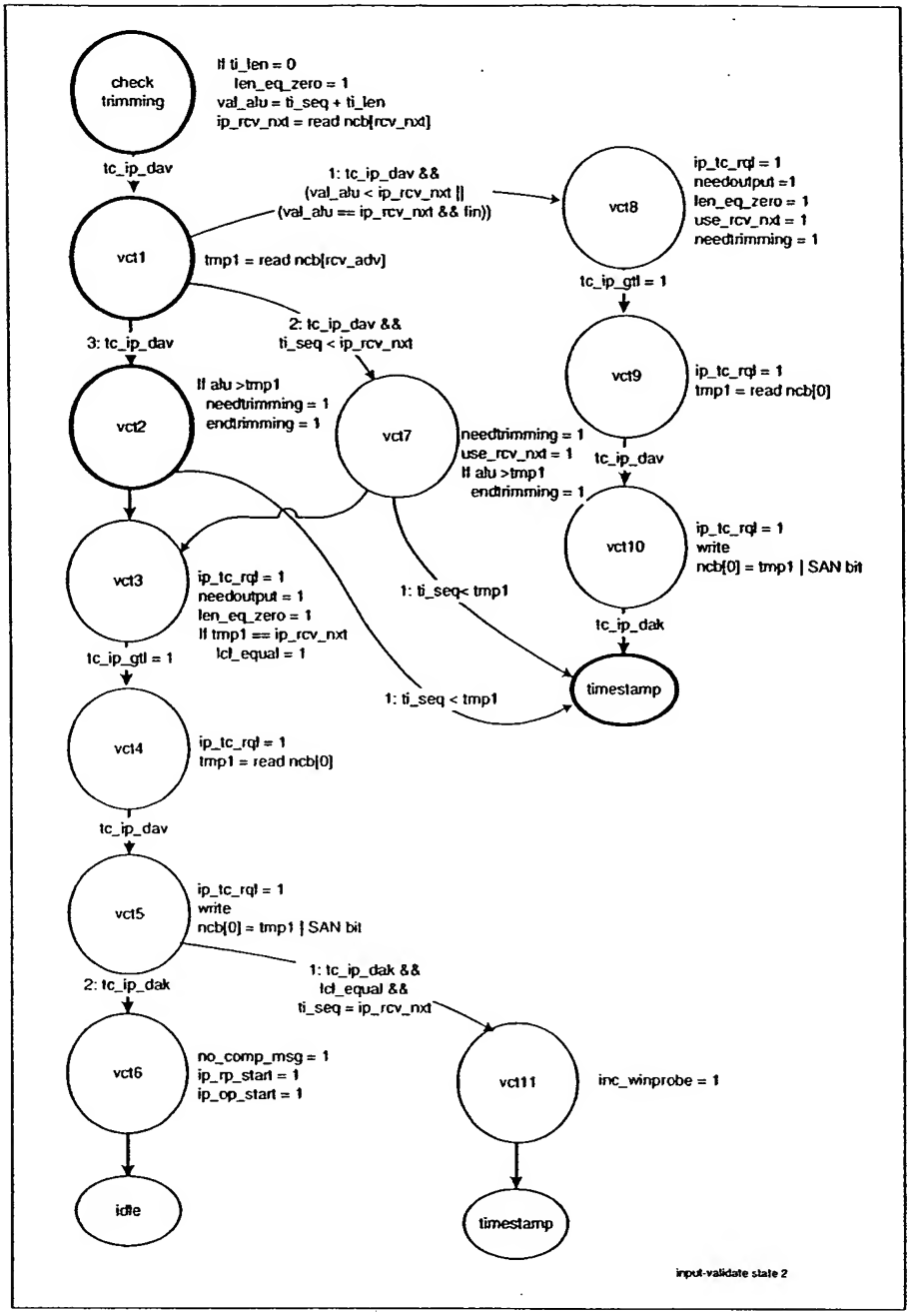

Figure 3C4: Validation State Machine for Trimming

17 857

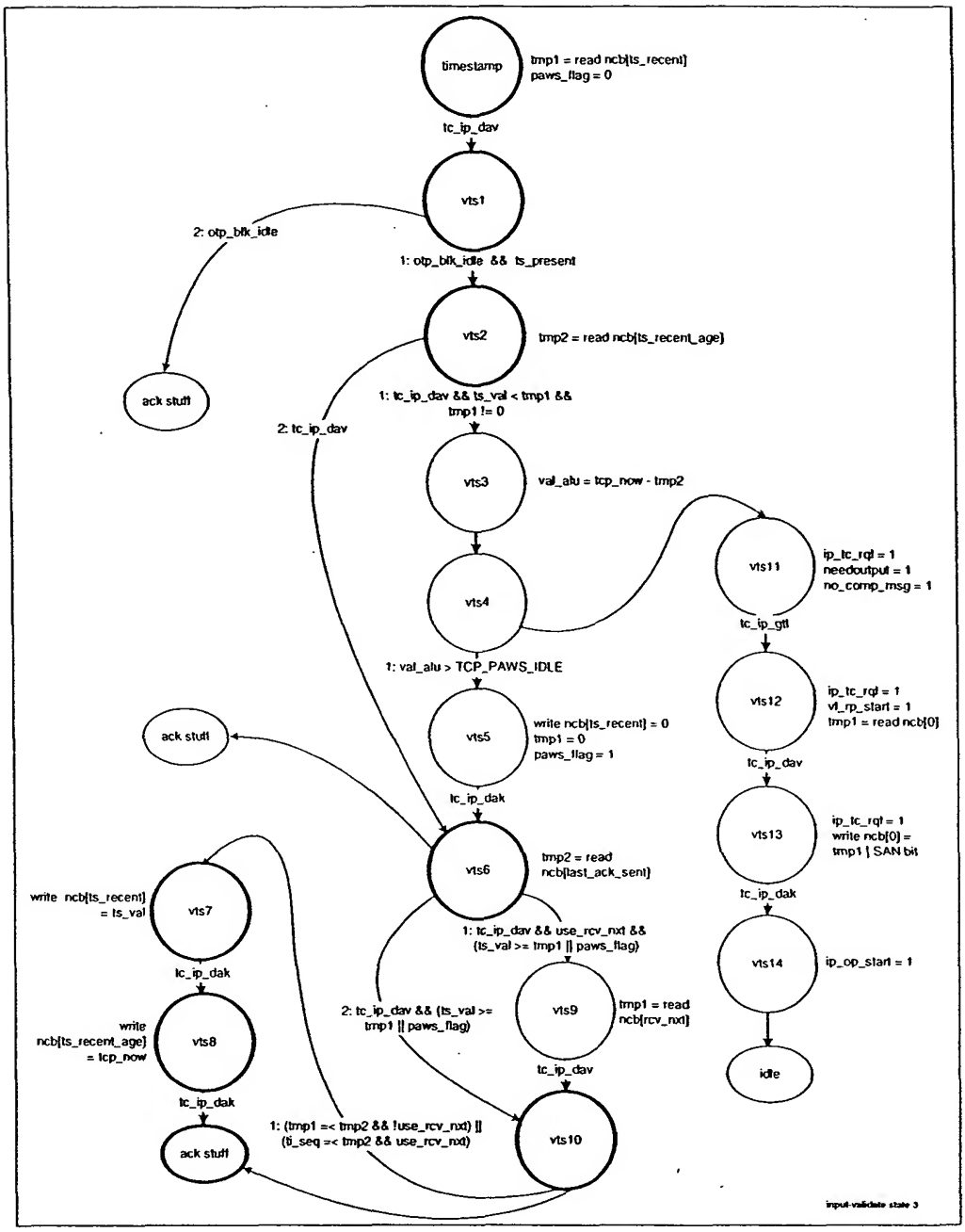

Figure 3C5: Validation State machine for Timestamp functionality

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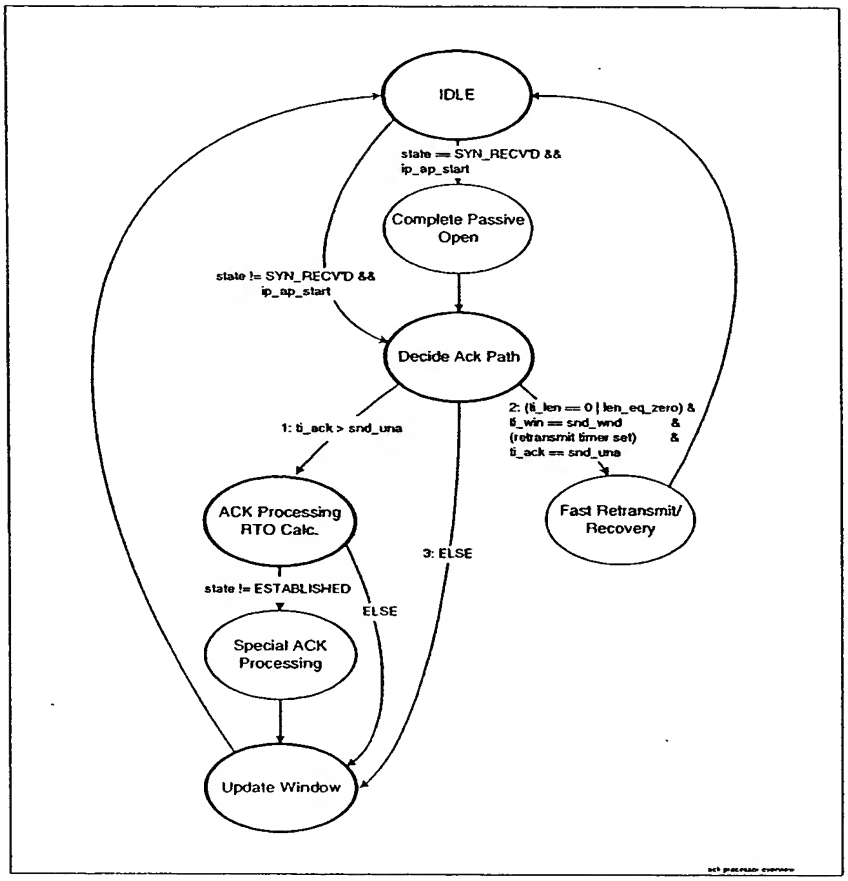

Figure3C6– ACK Processor

19 of 57

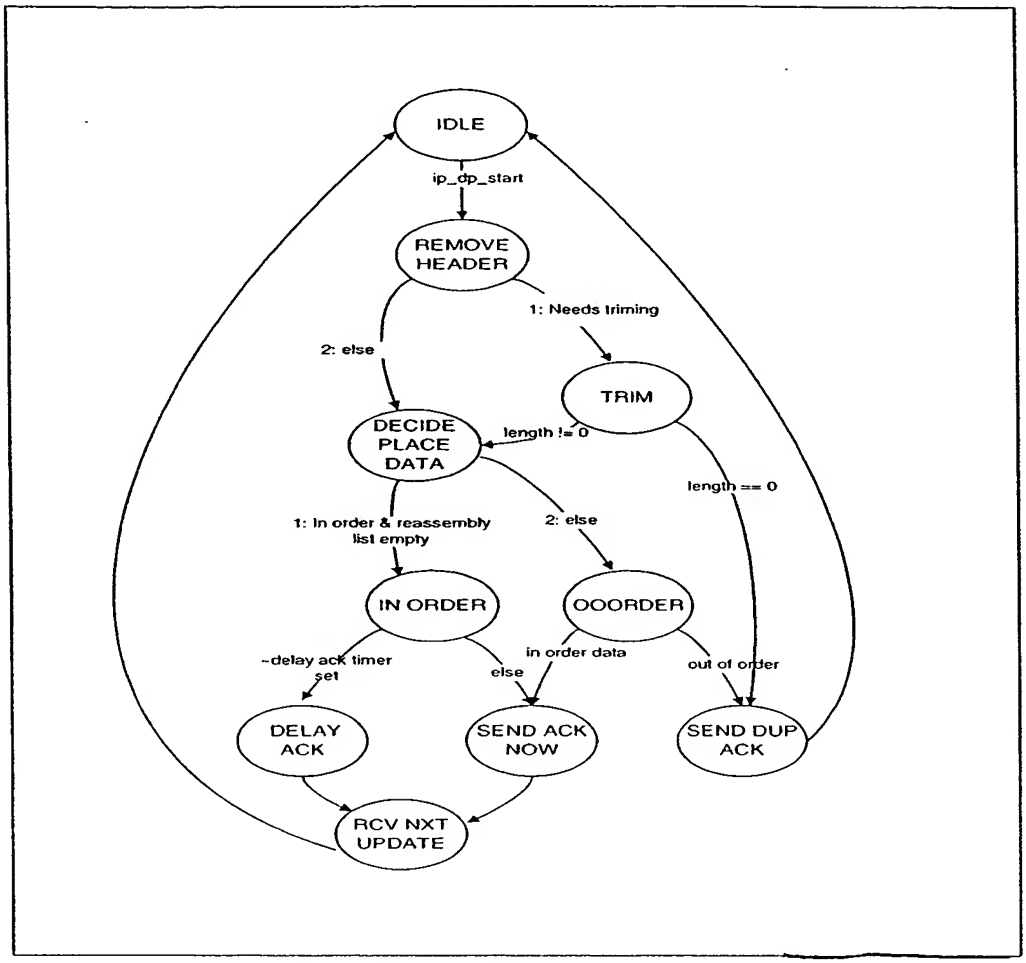

Figure 3C7 Data Processing State Machine

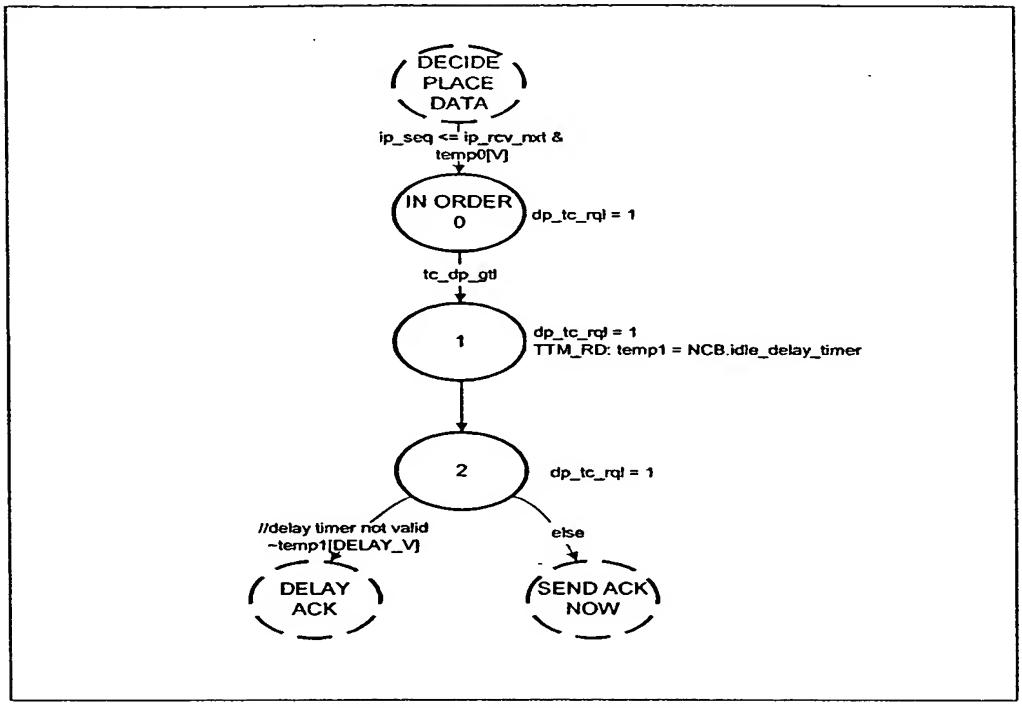

Figure 3C8 – Data Process Inorder

21951

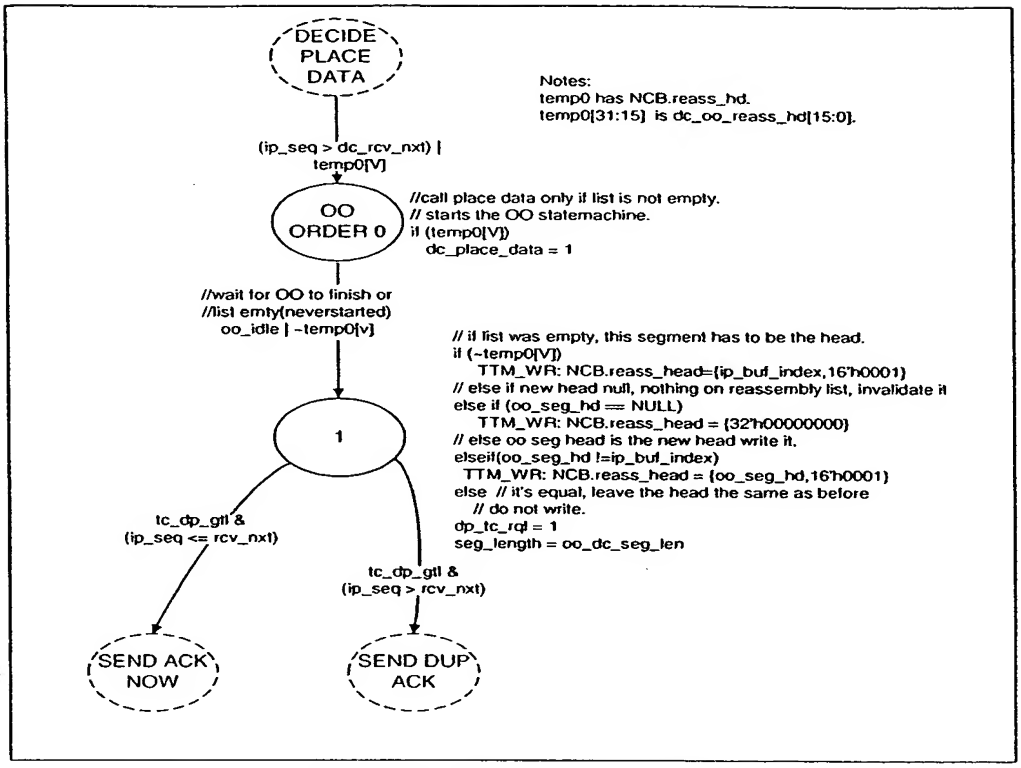

Figure 3C9 – Data Process Out of Order

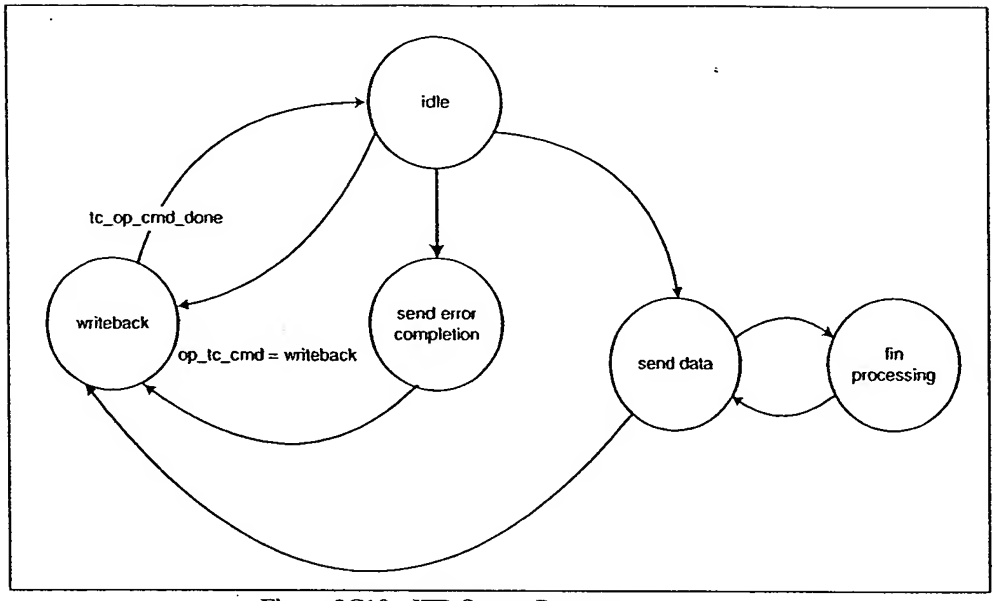

Figure 3C10 - ITP Output Processor f

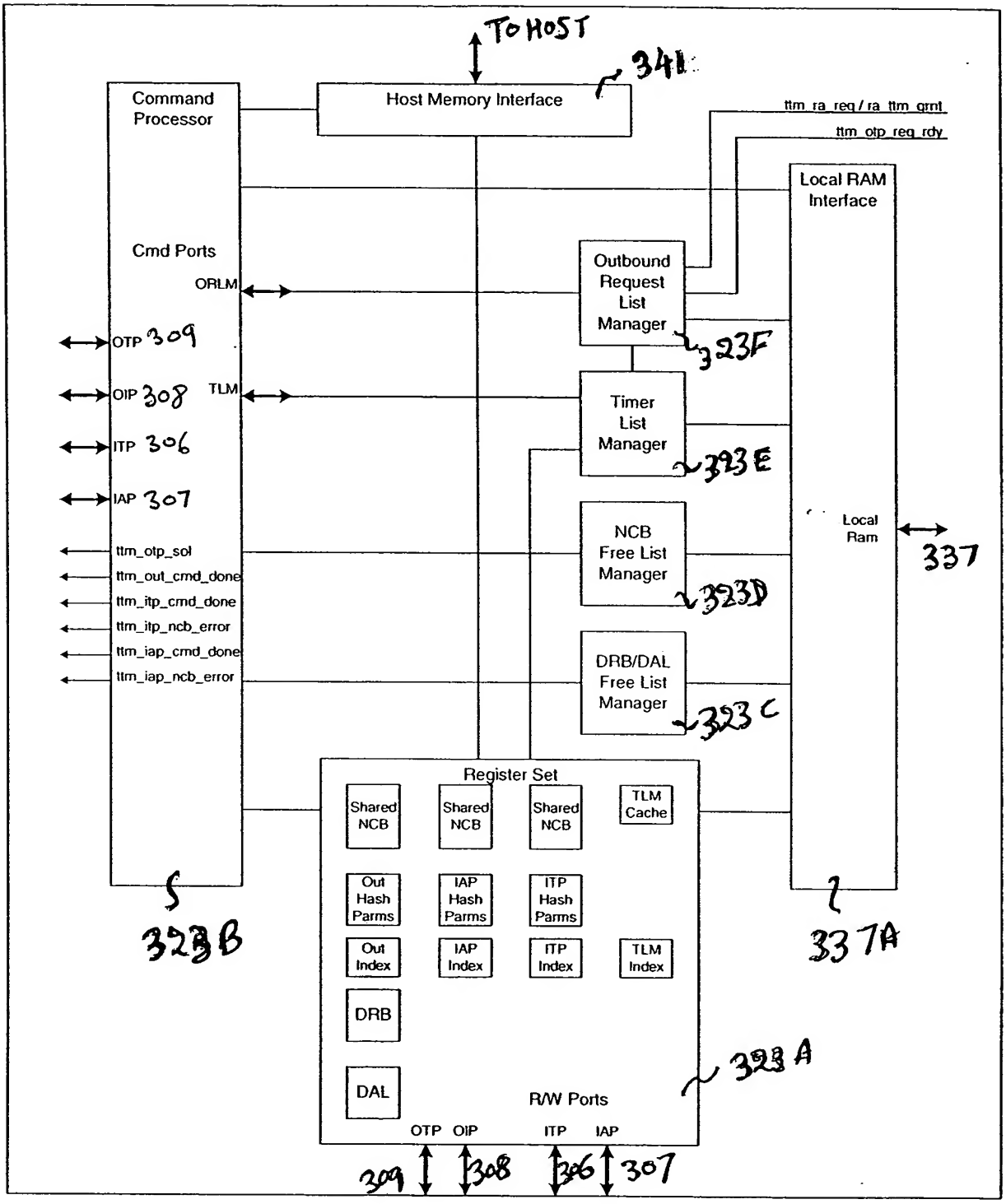

Figure 3D 1

323

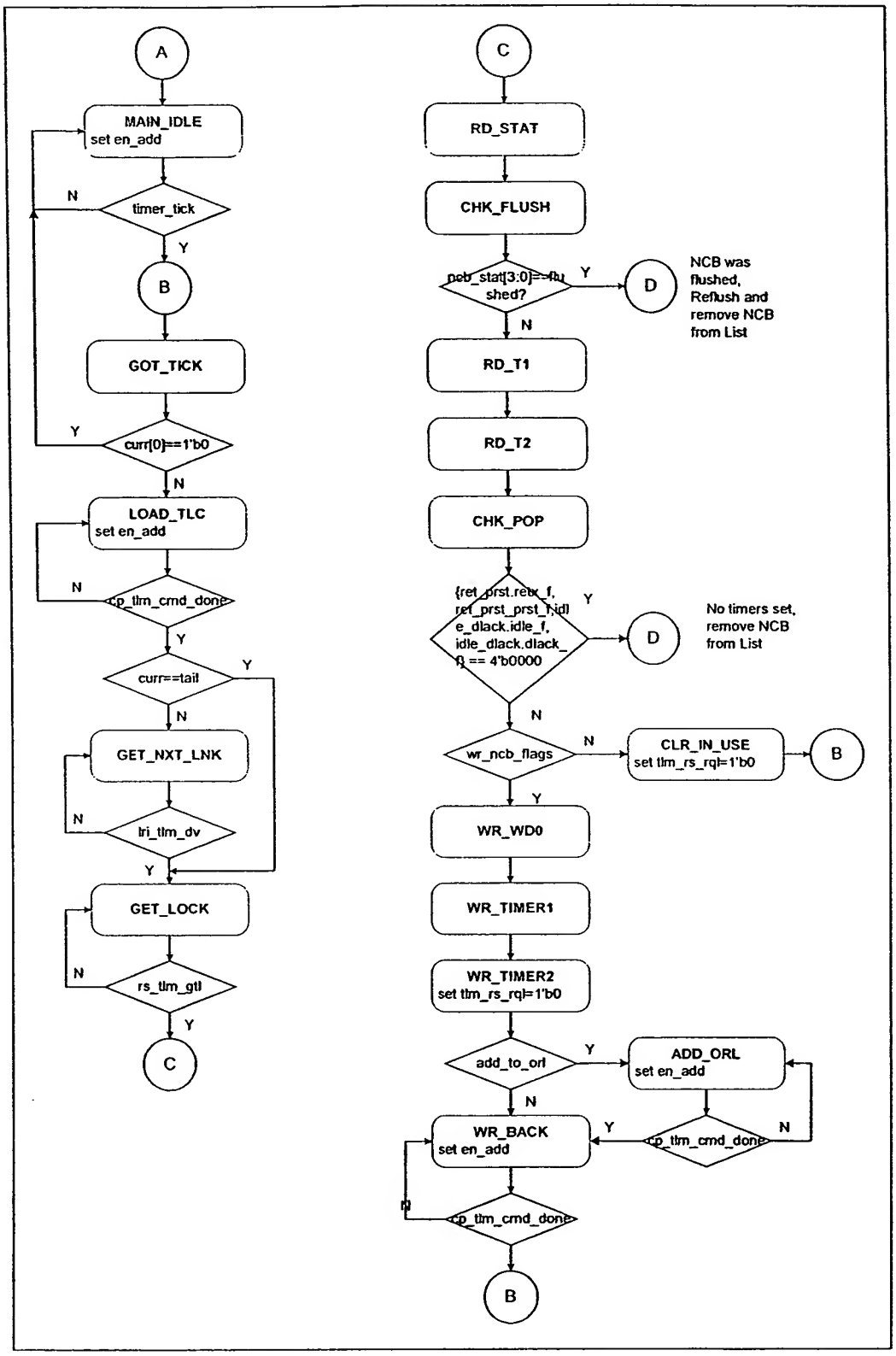

Figure 3D1 Timer List Manager State Machine

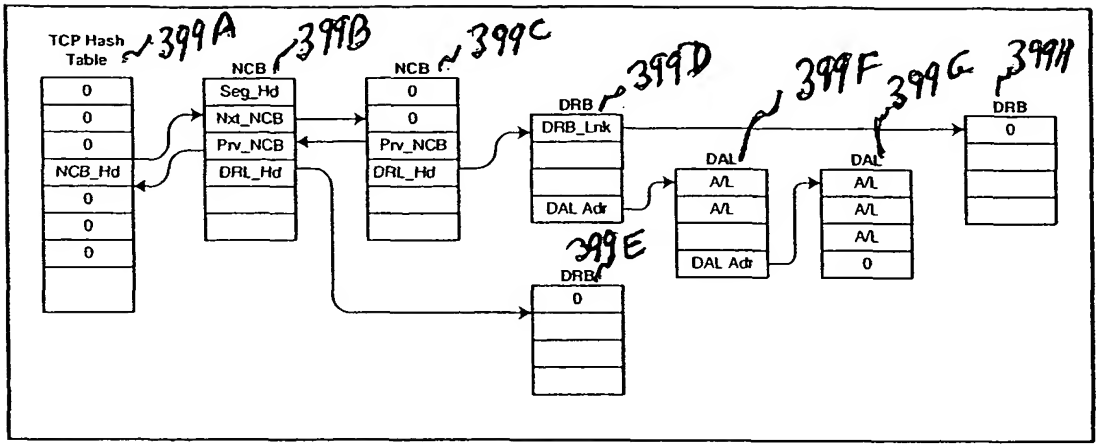

Figure 3E

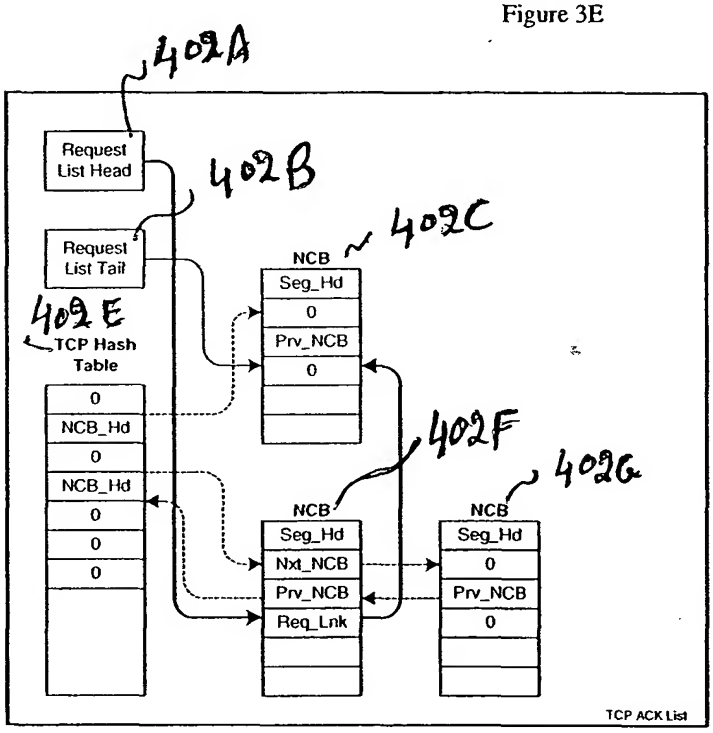

Figure 3F

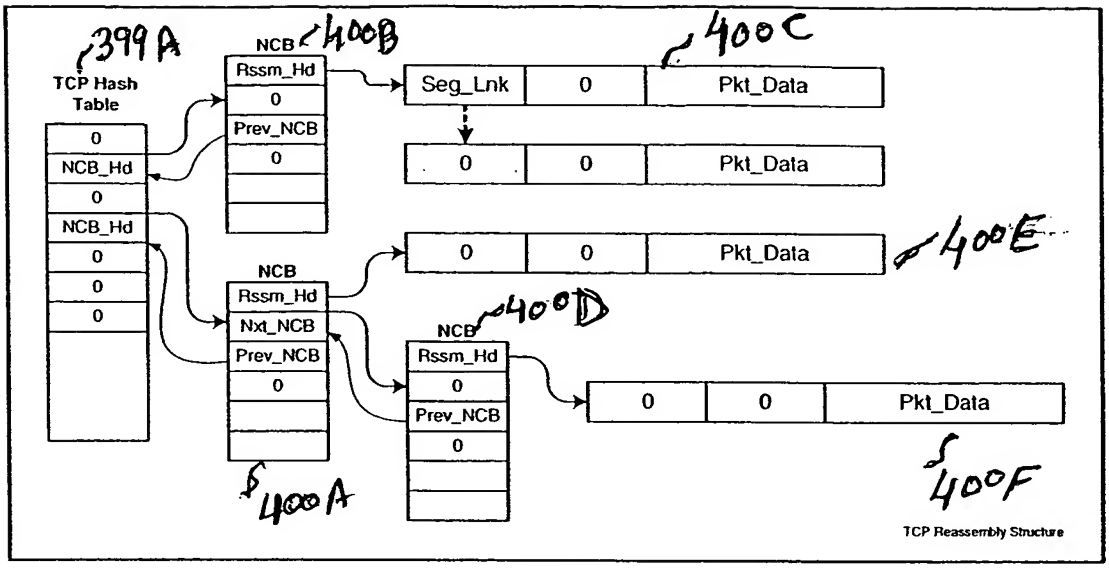

Figure 3G

400

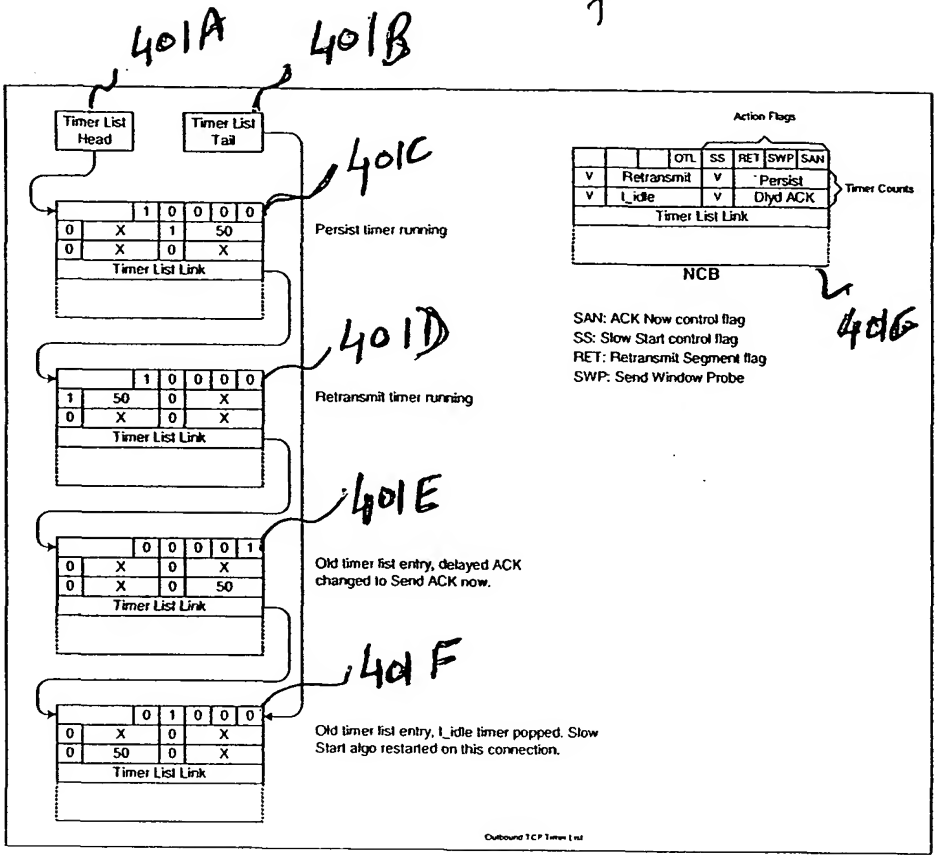

Figure 3H

401

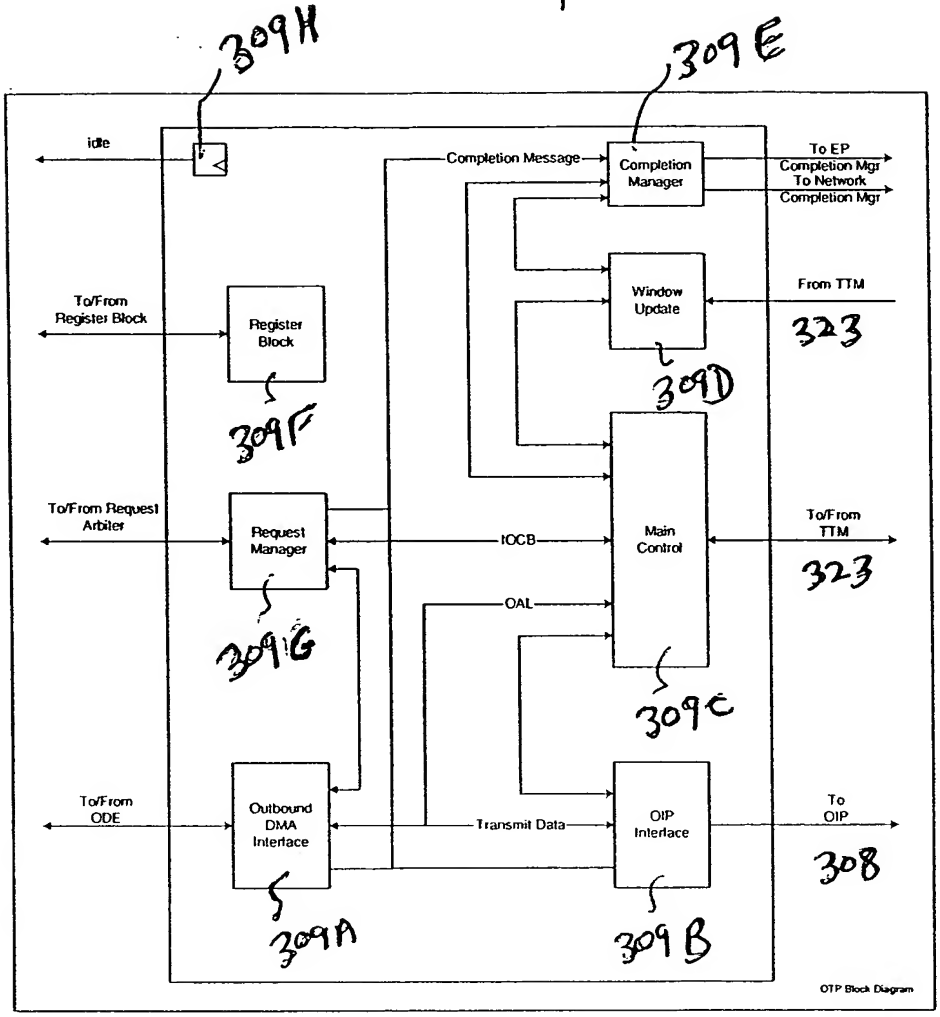

Figure 31

309

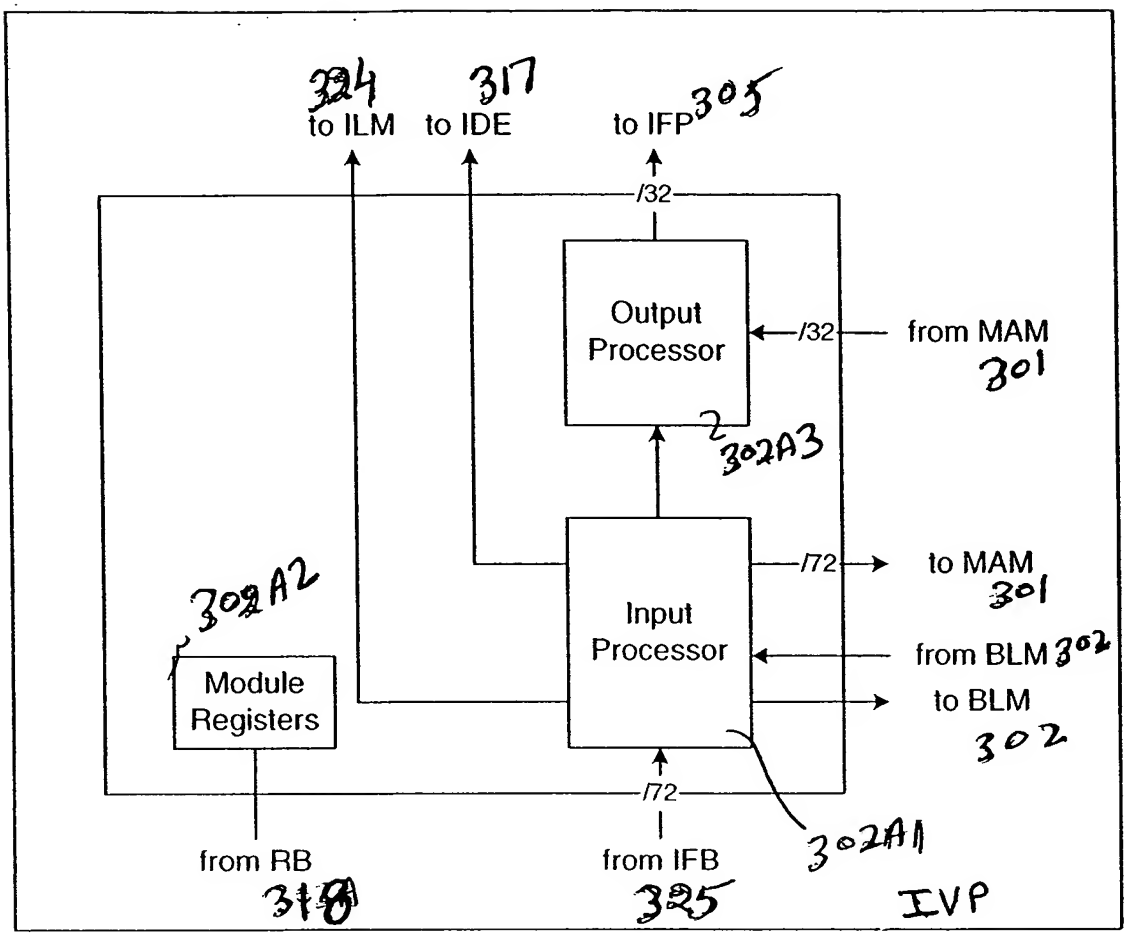

Figure 3J

302A

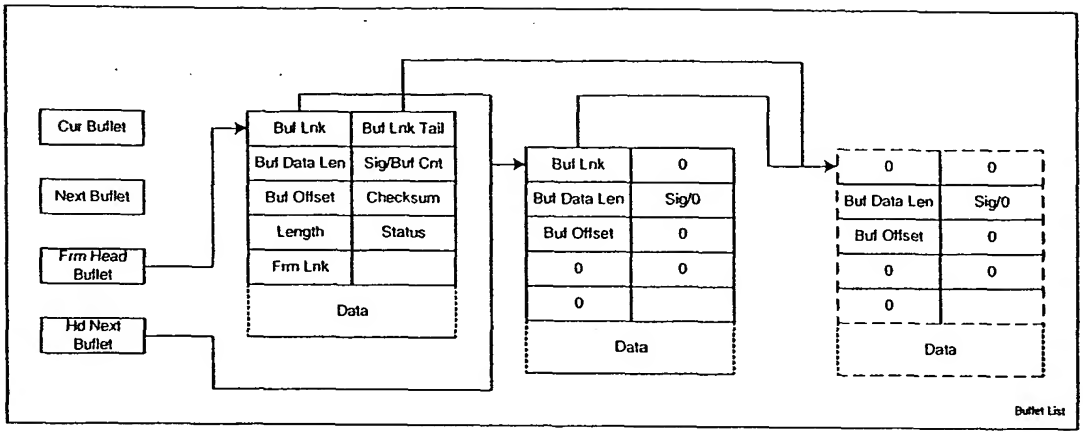

Figure 3J1 Buflet List Structure

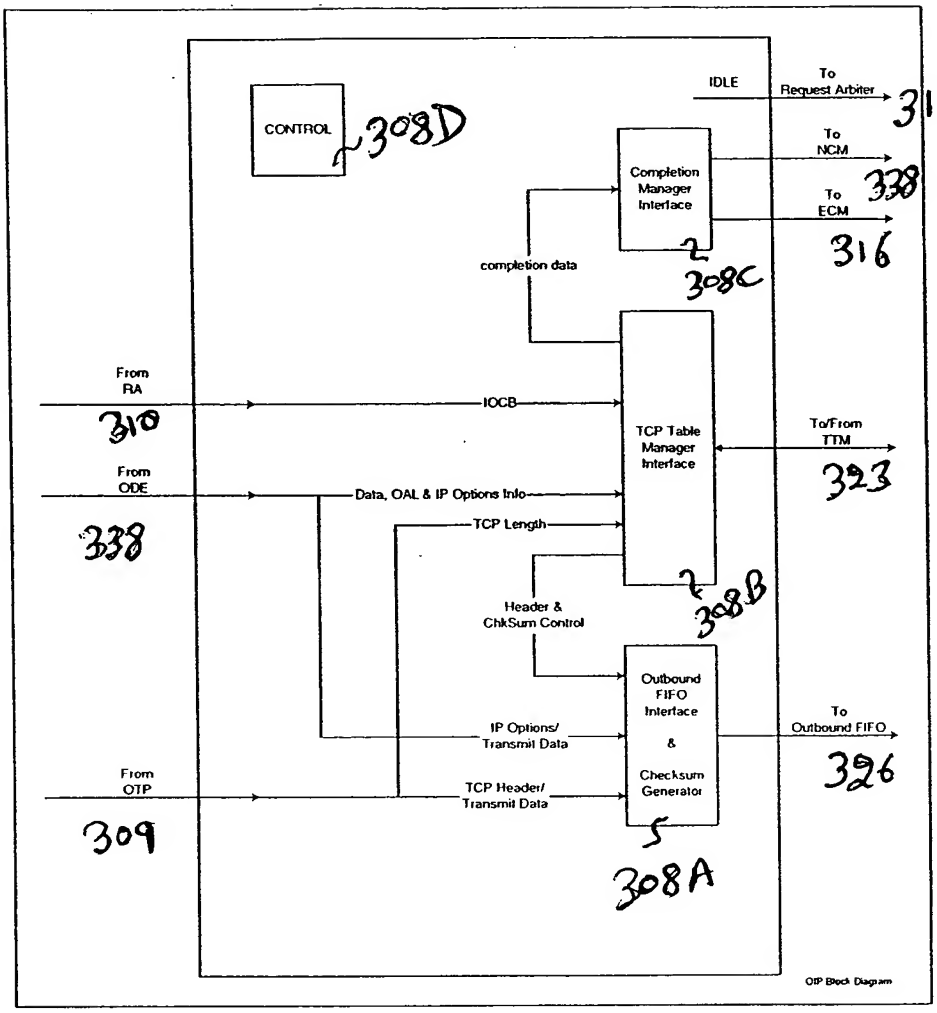

Figure 3K

308

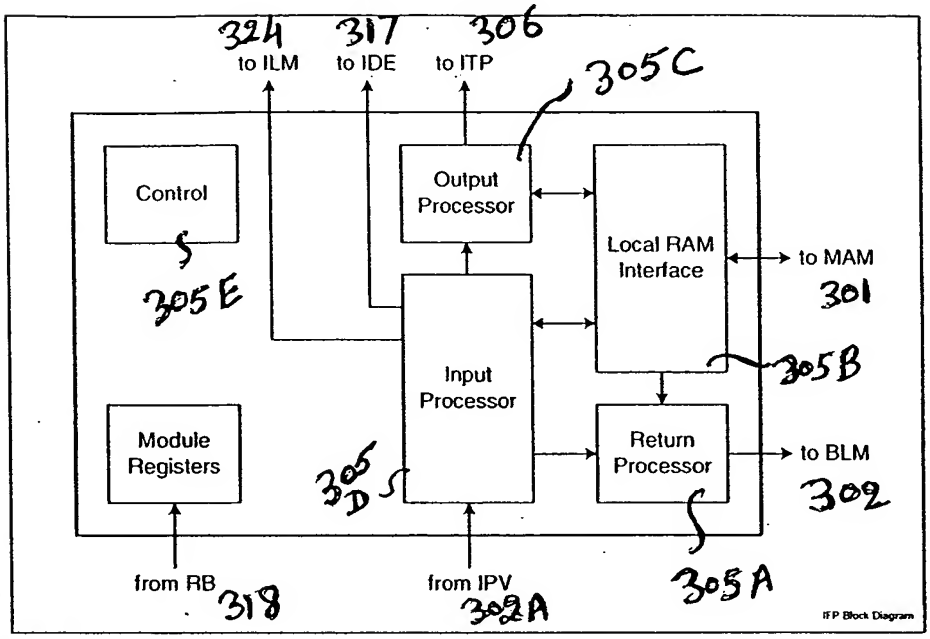

Figure 3L

305

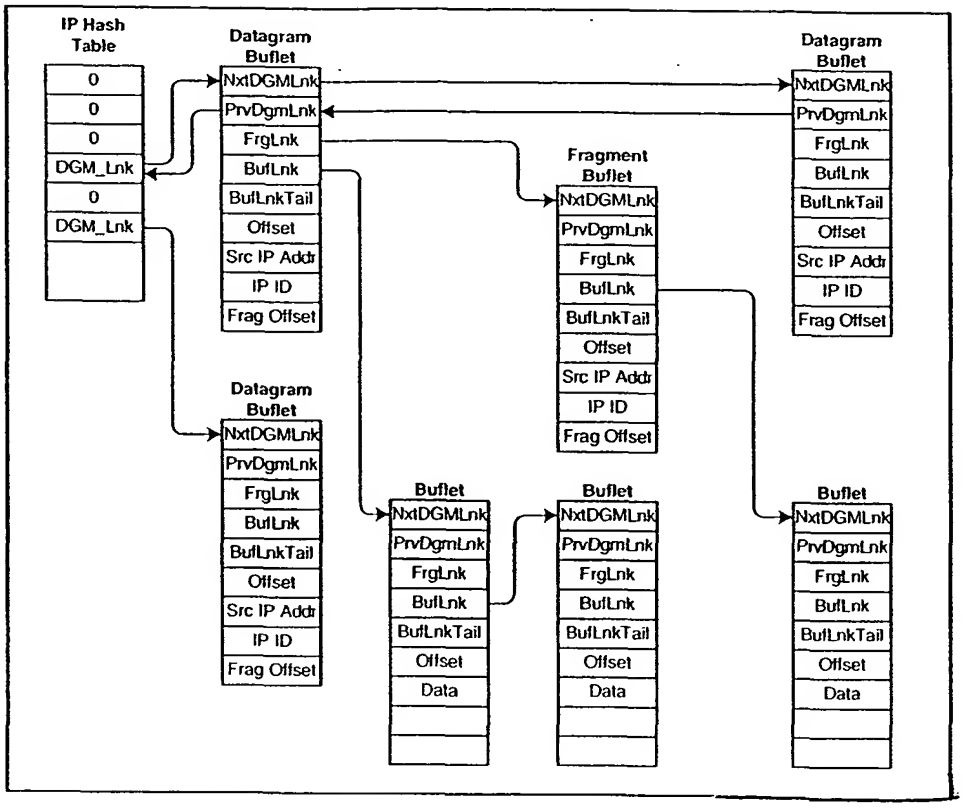
IP Hash Table
0
0
0
DGM_Lnk
0
DGM_Lnk
Datagram Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Src IP Addr
IP ID
Frag Offset
Datagram Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Src IP Addr
IP ID
Frag Offset
Fragment Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Src IP Addr
IP ID
Frag Offset
Datagram Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Src IP Addr
IP ID
Frag Offset
Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Data
Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Data
Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Data

Figure 3L1: -

34 of 51

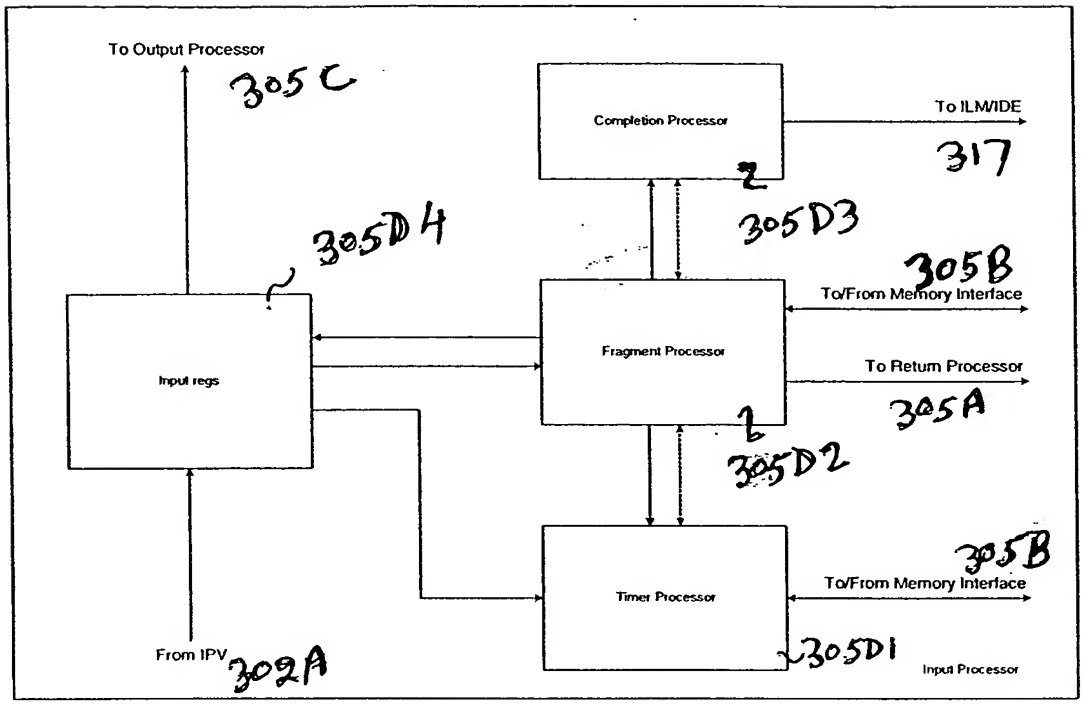

Figure 3L2

305D

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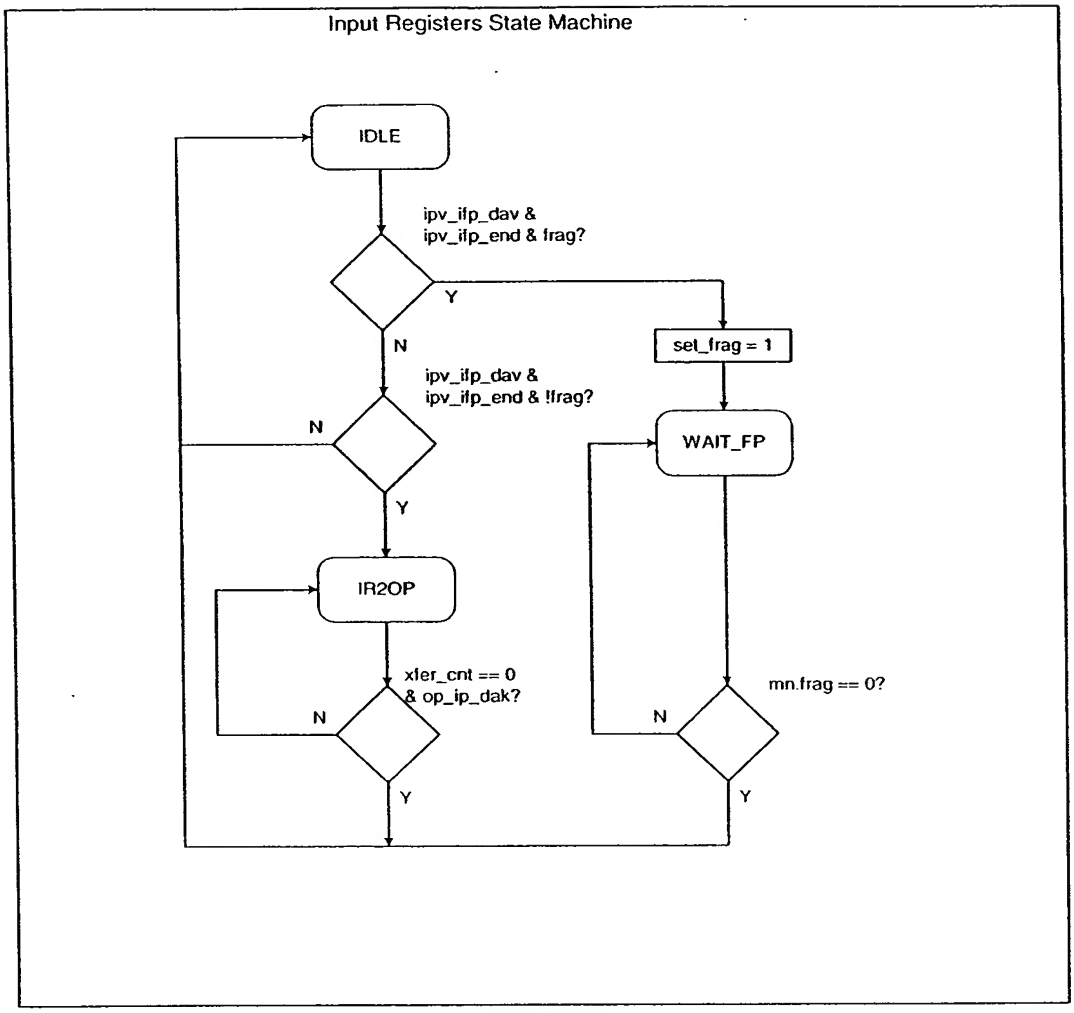

Figure 3L3

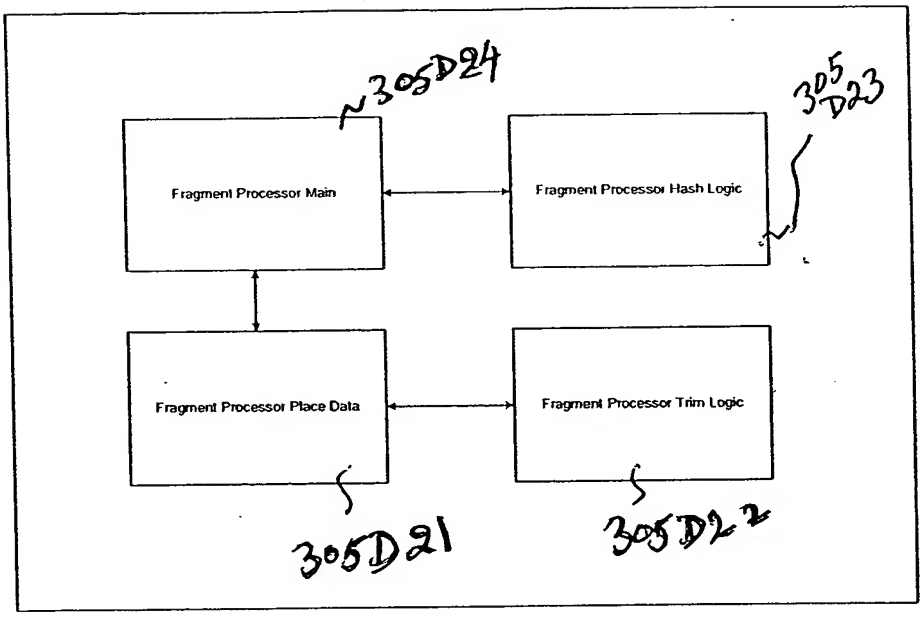

Figure 3L4

305D2

3 7 8 5 1

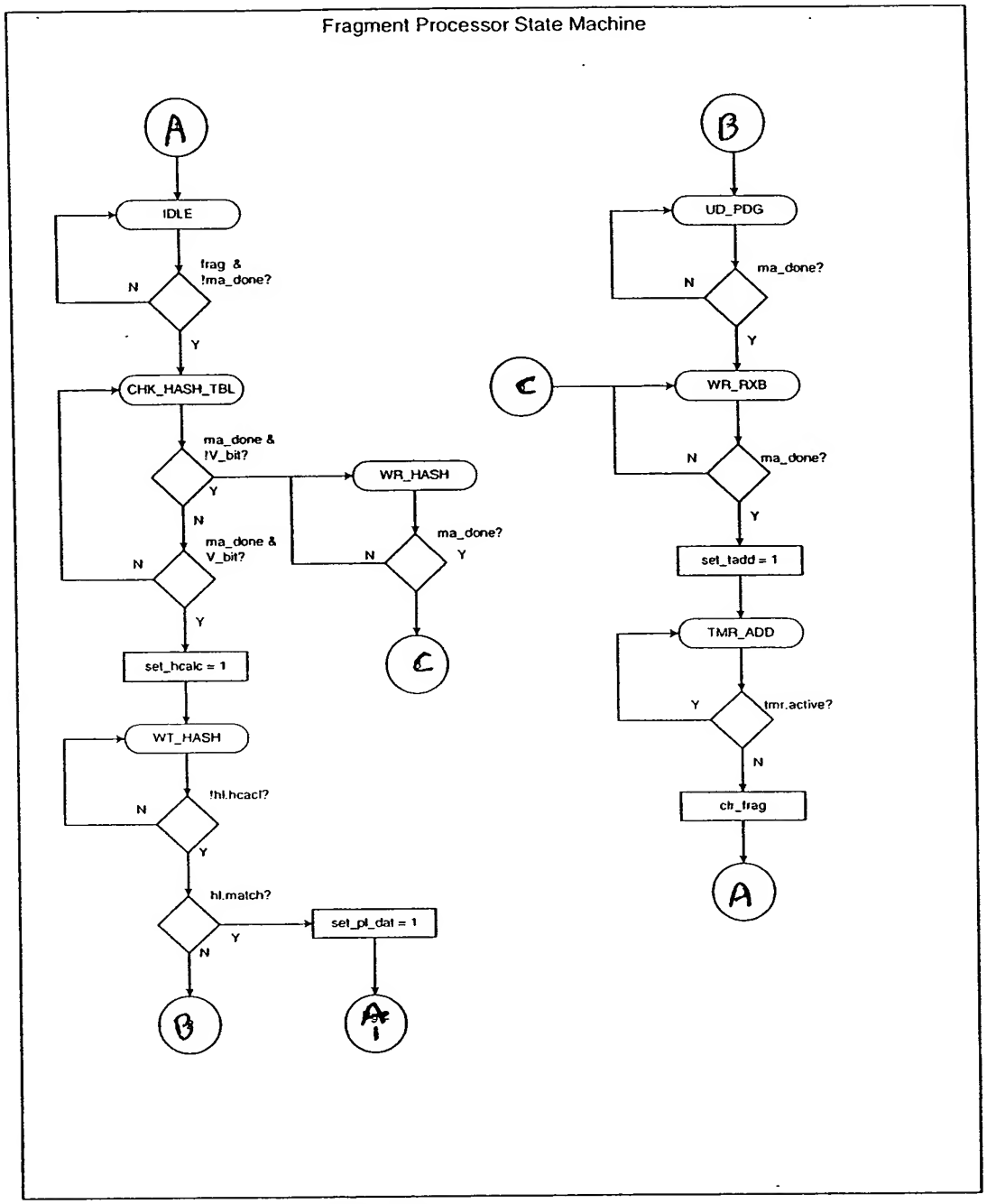

Figure 3L5A I

35 of 57

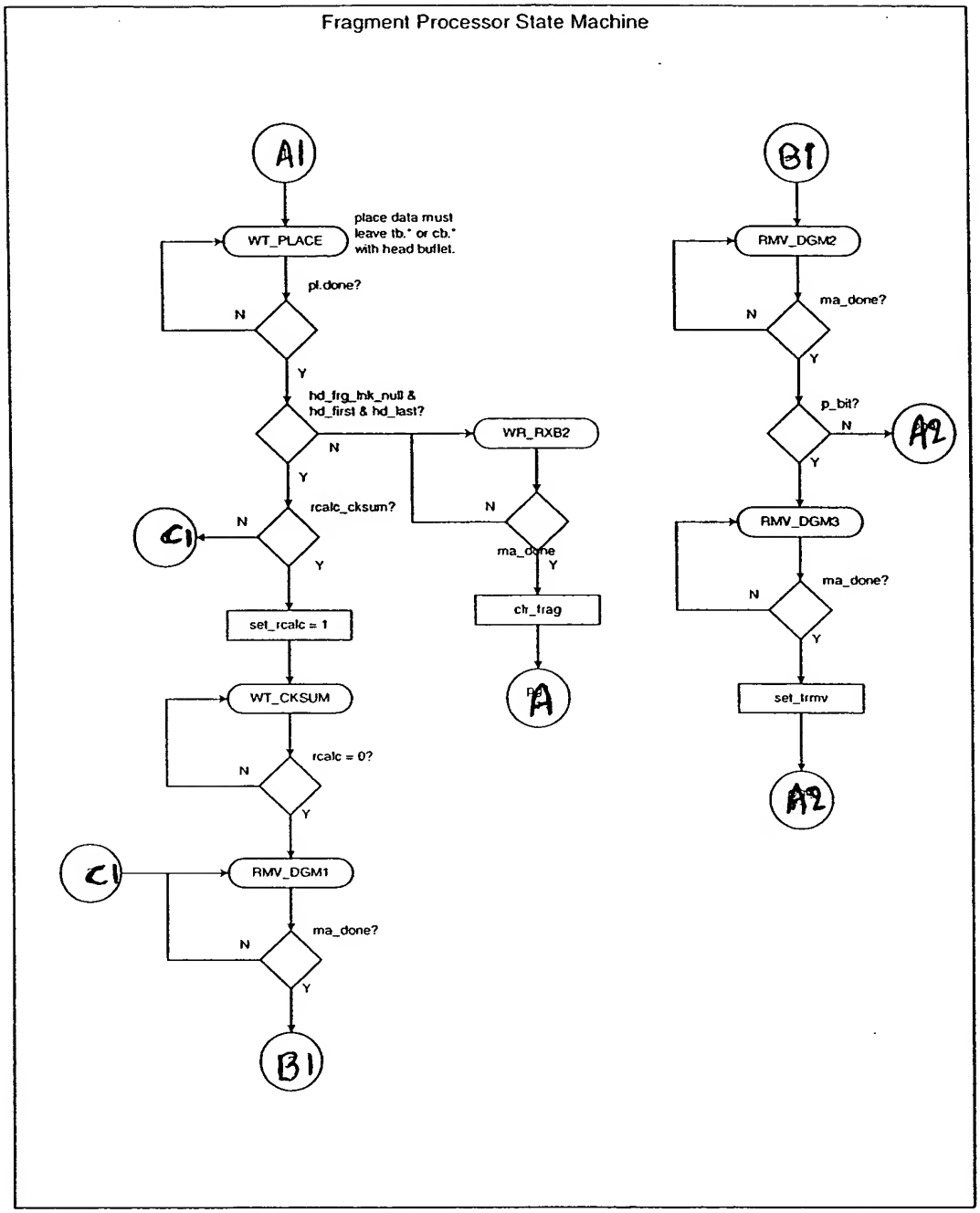

Figure 3L5B Fr

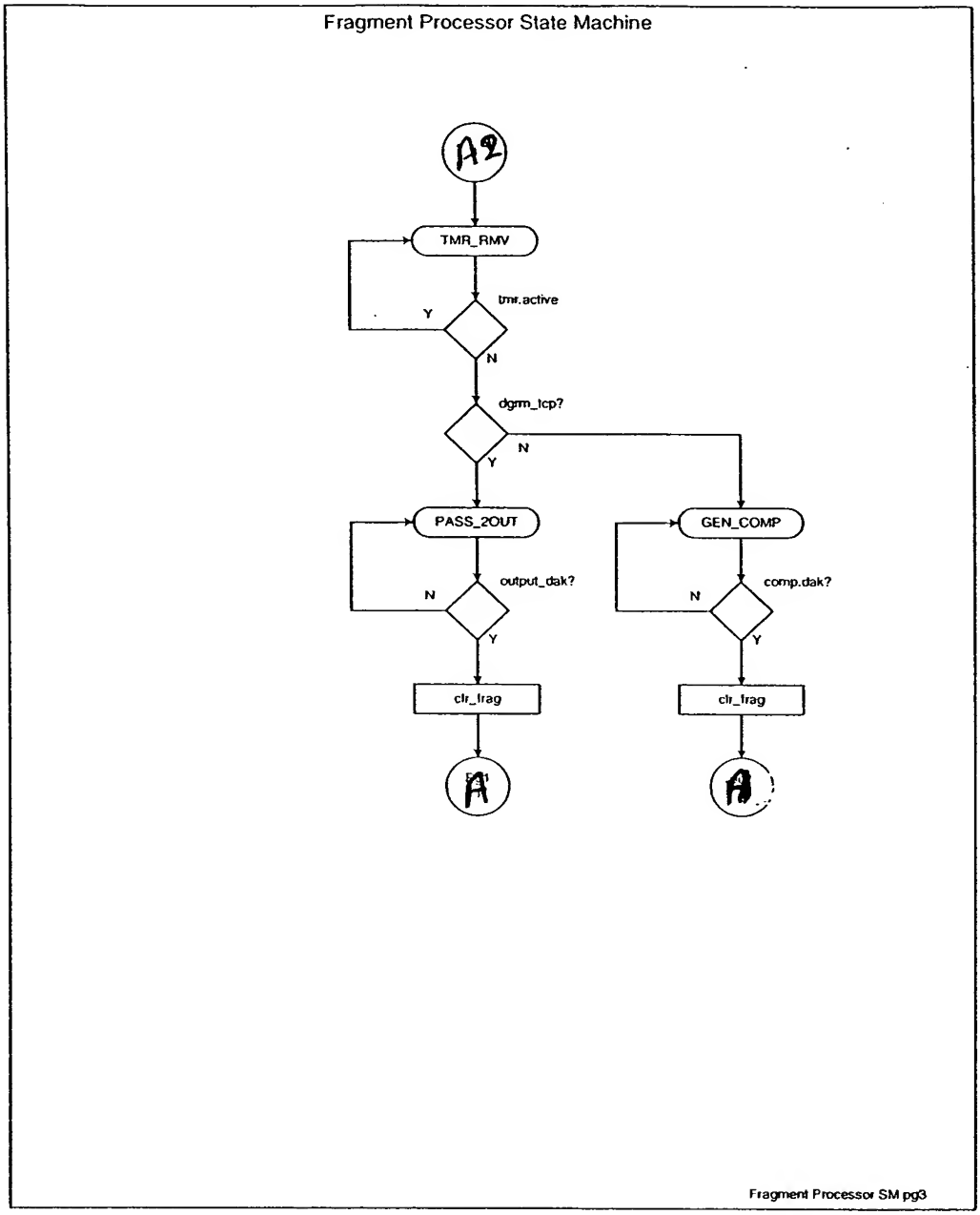
Fragment Processor State Machine
A2
TMR_RMV
tmr.active
Y
N
dgrm_tcp?
N
Y
PASS_2OUT
GEN_COMP
output_dak?
comp.dak?
N
N
Y
Y
clr_frag
clr_frag
A
A
Fragment Processor SM pg3

Figure 3L5C

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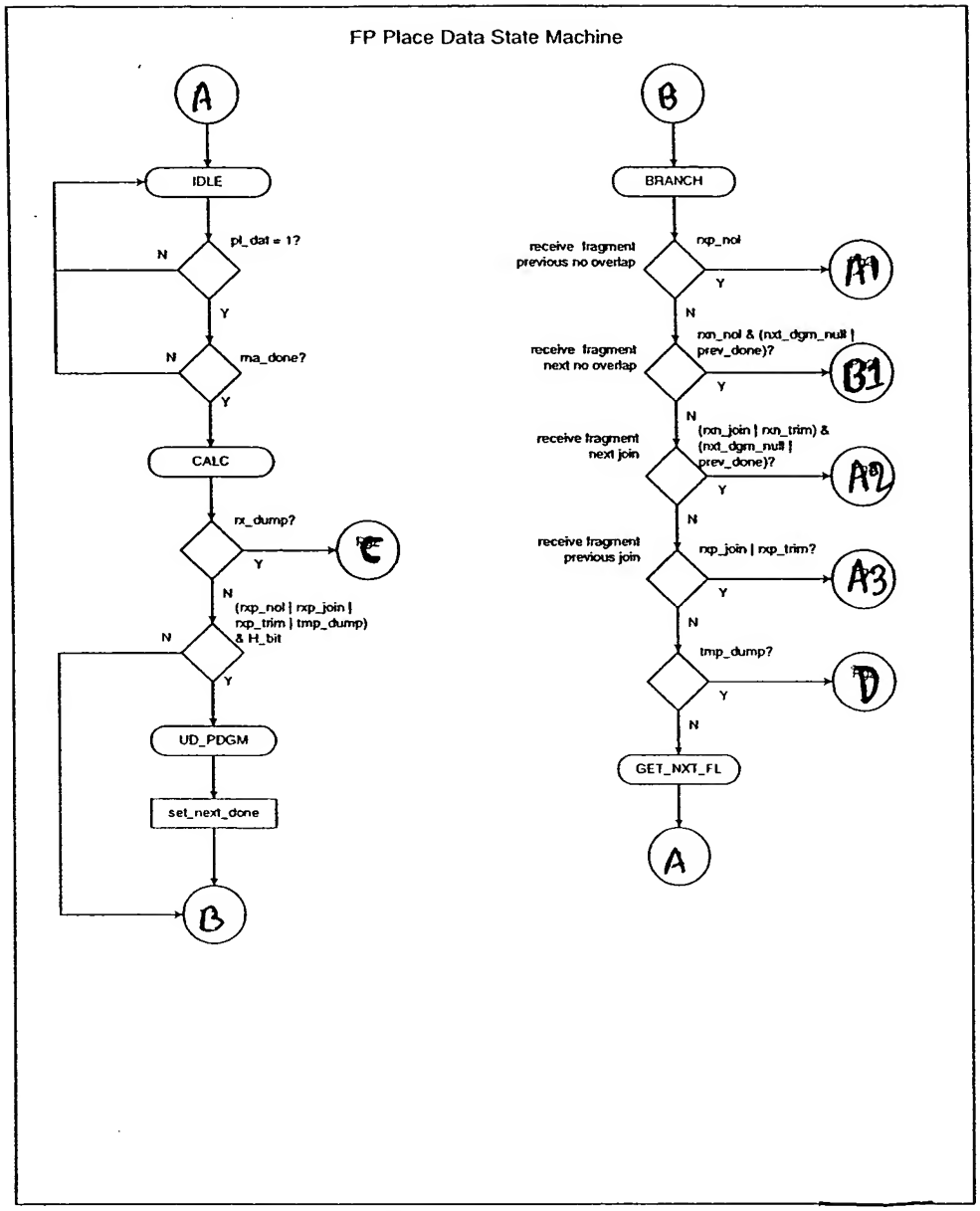

Figure 3L6A

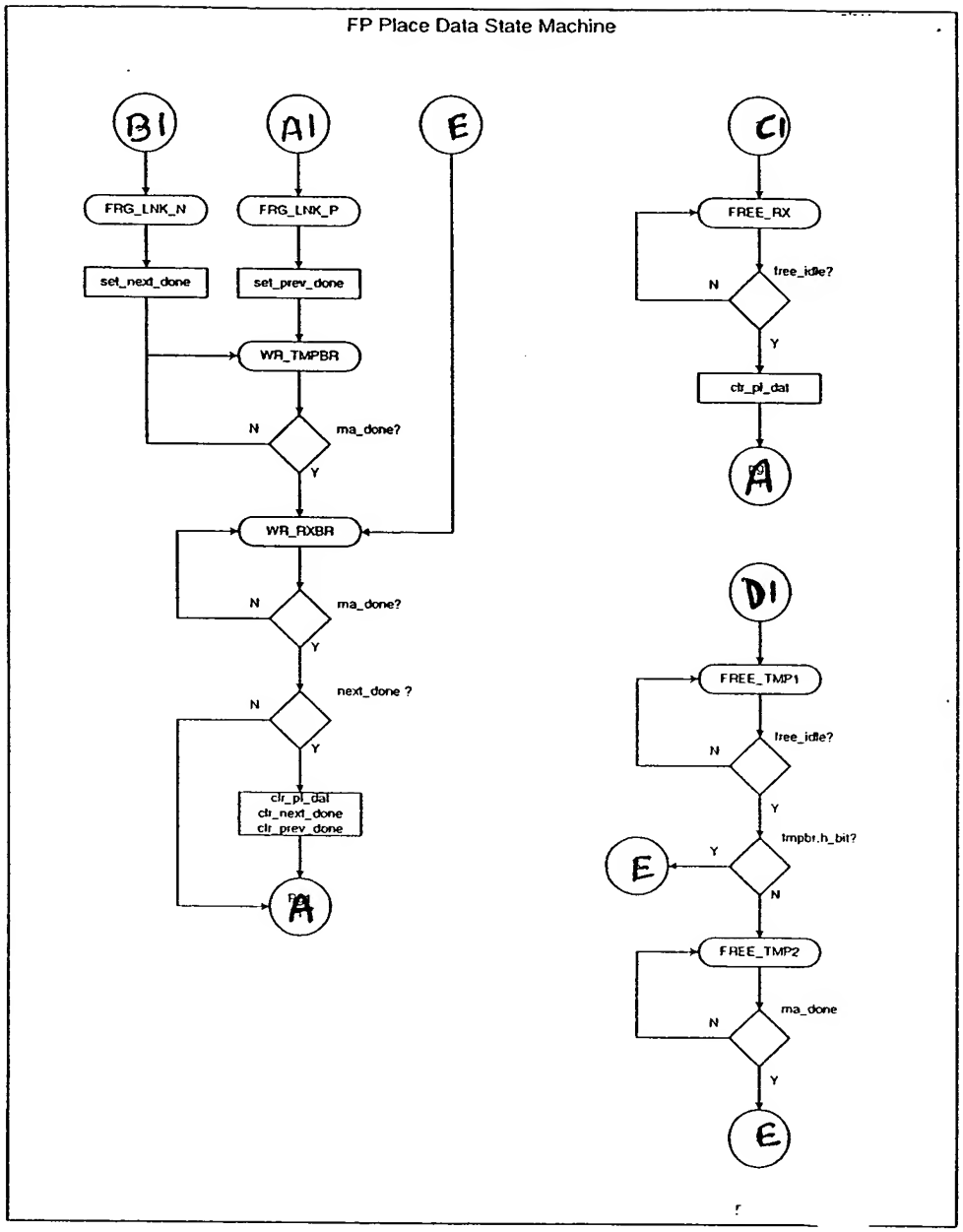
FP Place Data State Machine
B1
A1
E
C1
D1
FRG_LNK_N
FRG_LNK_P
set_next_done
set_prev_done
WR_TMPBR
ma_done?
N
Y
WR_RXBR
ma_done?
next_done ?
clr_pl_dat
clr_next_done
clr_prev_done
A
FREE_RX
free_idle?
clr_pl_dat
FREE_TMP1
free_idle?
tmpbr.h_bit?
FREE_TMP2
ma_done
E

Figure 3L6 B

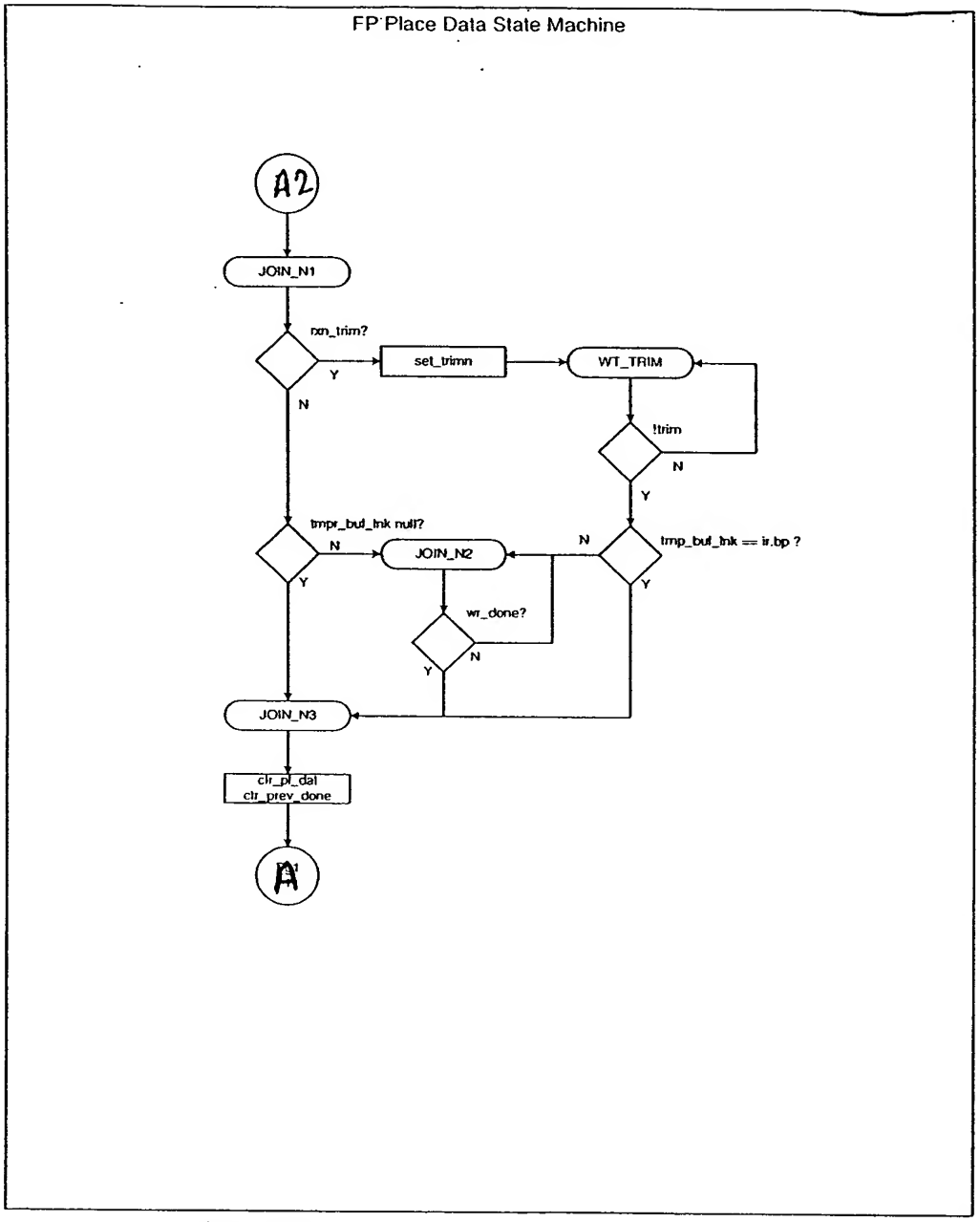
FP Place Data State Machine
A2
JOIN_N1
non_trim?
Y
N
set_trimn
WT_TRIM
!trim
N
Y
tmpr_bud_lnk null?
N
Y
JOIN_N2
N
tmp_buf_lnk == ir.bp ?
Y
wr_done?
Y
N
JOIN_N3
clr_pl_dal
clr_prev_done
A1

Figure 3L6C

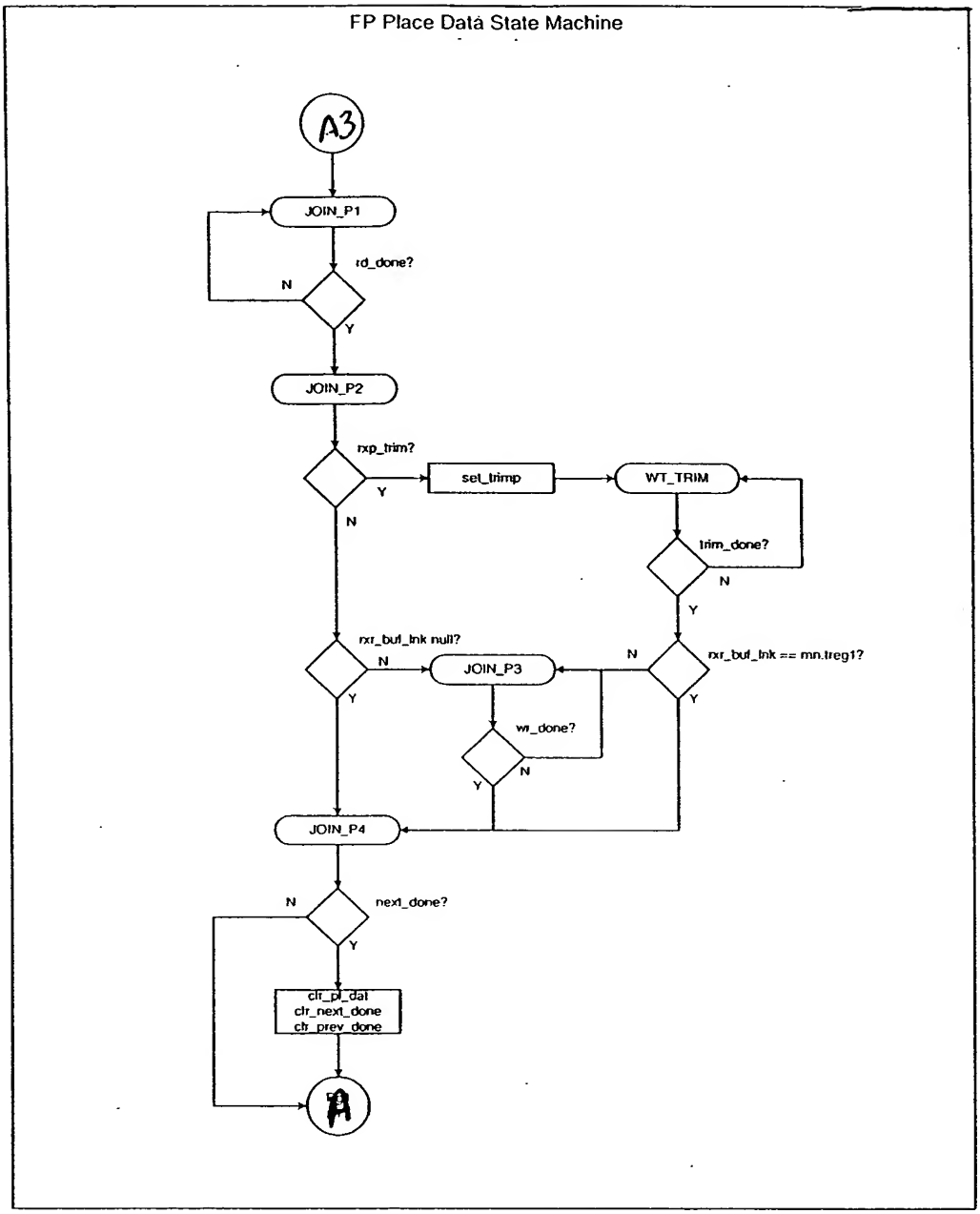
FP Place Data State Machine
A3
JOIN_P1
rd_done?
N
Y
JOIN_P2
rxp_trim?
Y
set_trimp
WT_TRIM
N
trim_done?
N
Y
rxr_buf_lnk null?
N
JOIN_P3
N
rxr_buf_lnk == mn.treg1?
Y
Y
wt_done?
Y
N
JOIN_P4
N
next_done?
Y
clr_pl_dat
clr_next_done
clr_prev_done
A

Figure 3L6D

44757

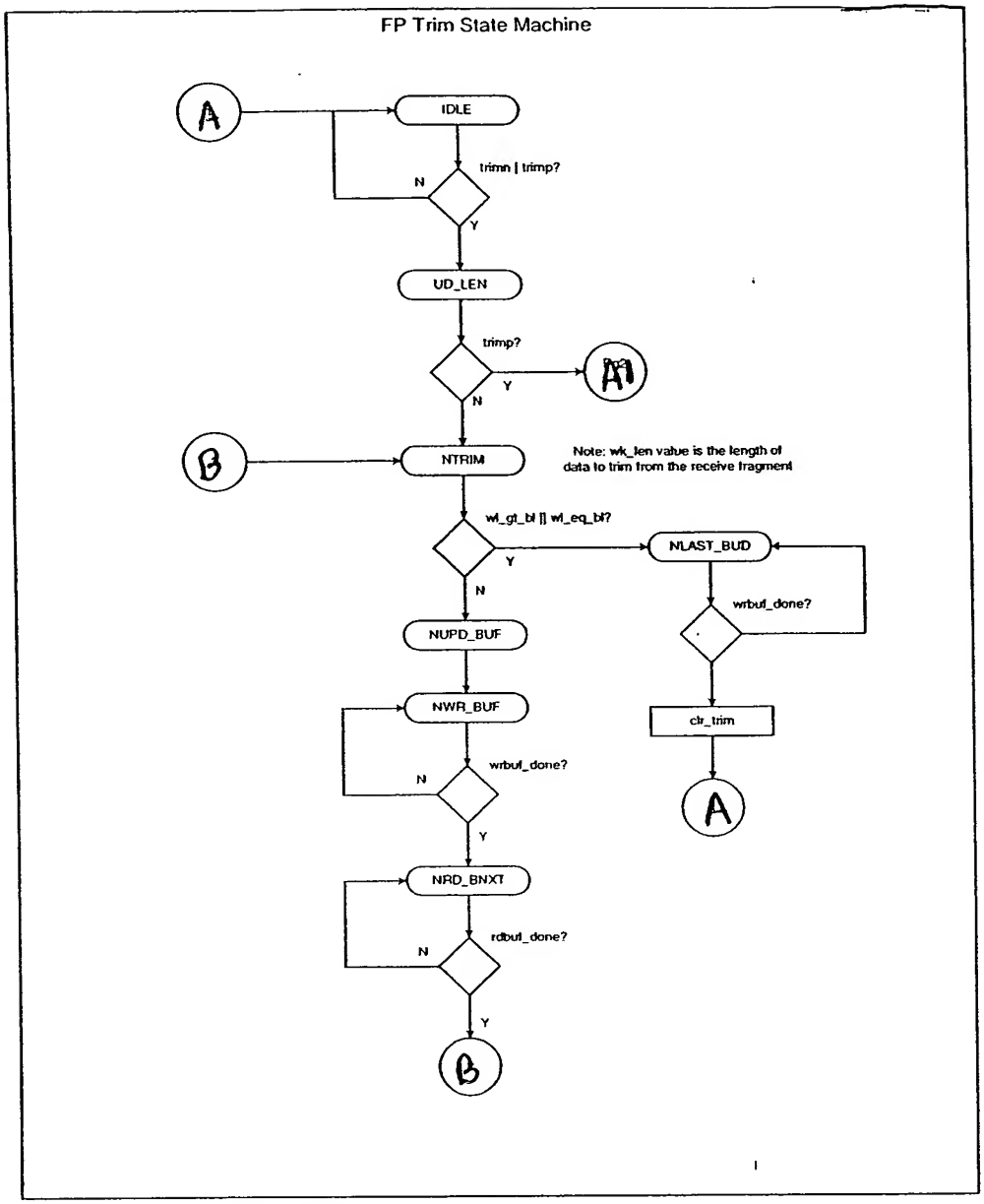

Figure 3L7A

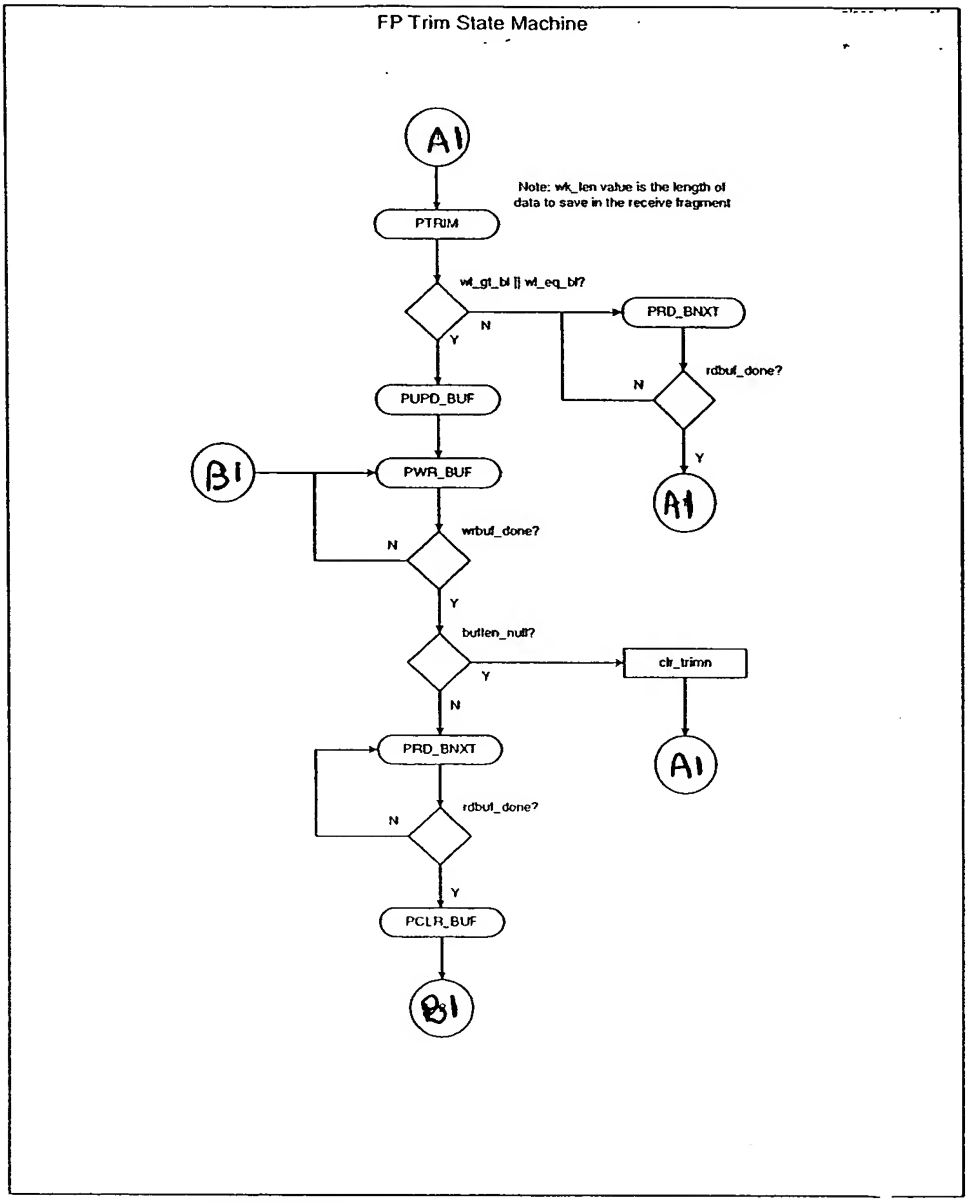
FP Trim State Machine
A1
Note: wk_len value is the length of data to save in the receive fragment
PTRIM
wl_gt_bl || wl_eq_bl?
N
Y
PRD_BNXT
rdbuf_done?
N
Y
A1
PUPD_BUF
B1
PWR_BUF
wrbuf_done?
N
Y
buflen_null?
Y
clr_trimn
N
A1
PRD_BNXT
rdbuf_done?
N
Y
PCLR_BUF
B1

Figure 3L7B:

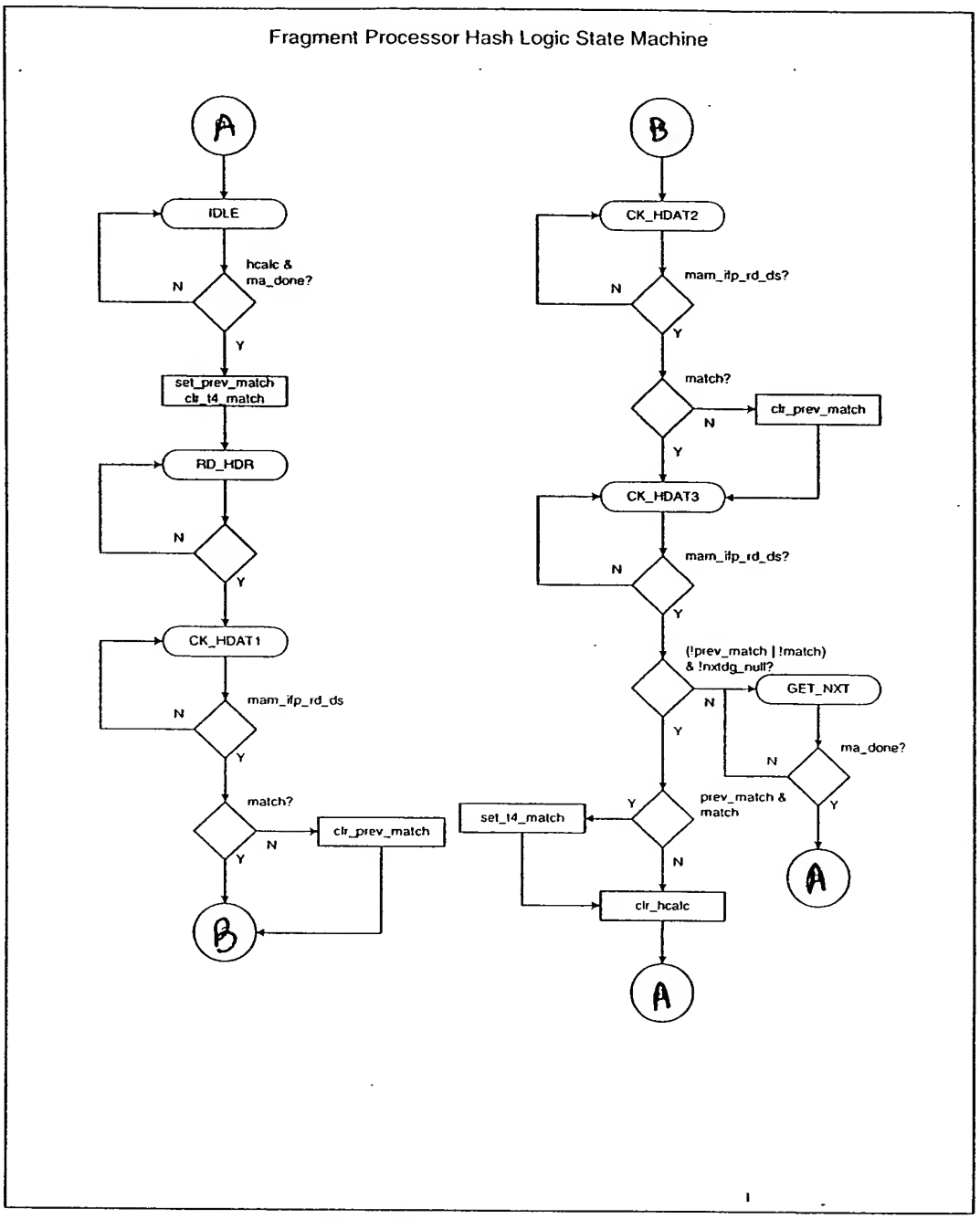
Fragment Processor Hash Logic State Machine
A
IDLE
hcalc &
ma_done?
N
Y
set_prev_match
clr_t4_match
RD_HDR
N
Y
CK_HDAT1
mam_ifp_rd_ds
N
Y
match?
clr_prev_match
N
Y
B
B
CK_HDAT2
mam_ifp_rd_ds?
N
Y
match?
clr_prev_match
N
Y
CK_HDAT3
mam_ifp_rd_ds?
N
Y
(!prev_match | !match)
& !nxtdg_null?
GET_NXT
N
Y
ma_done?
N
Y
A
prev_match &
match
Y
set_t4_match
N
clr_hcalc
A

Figure 3L8 1

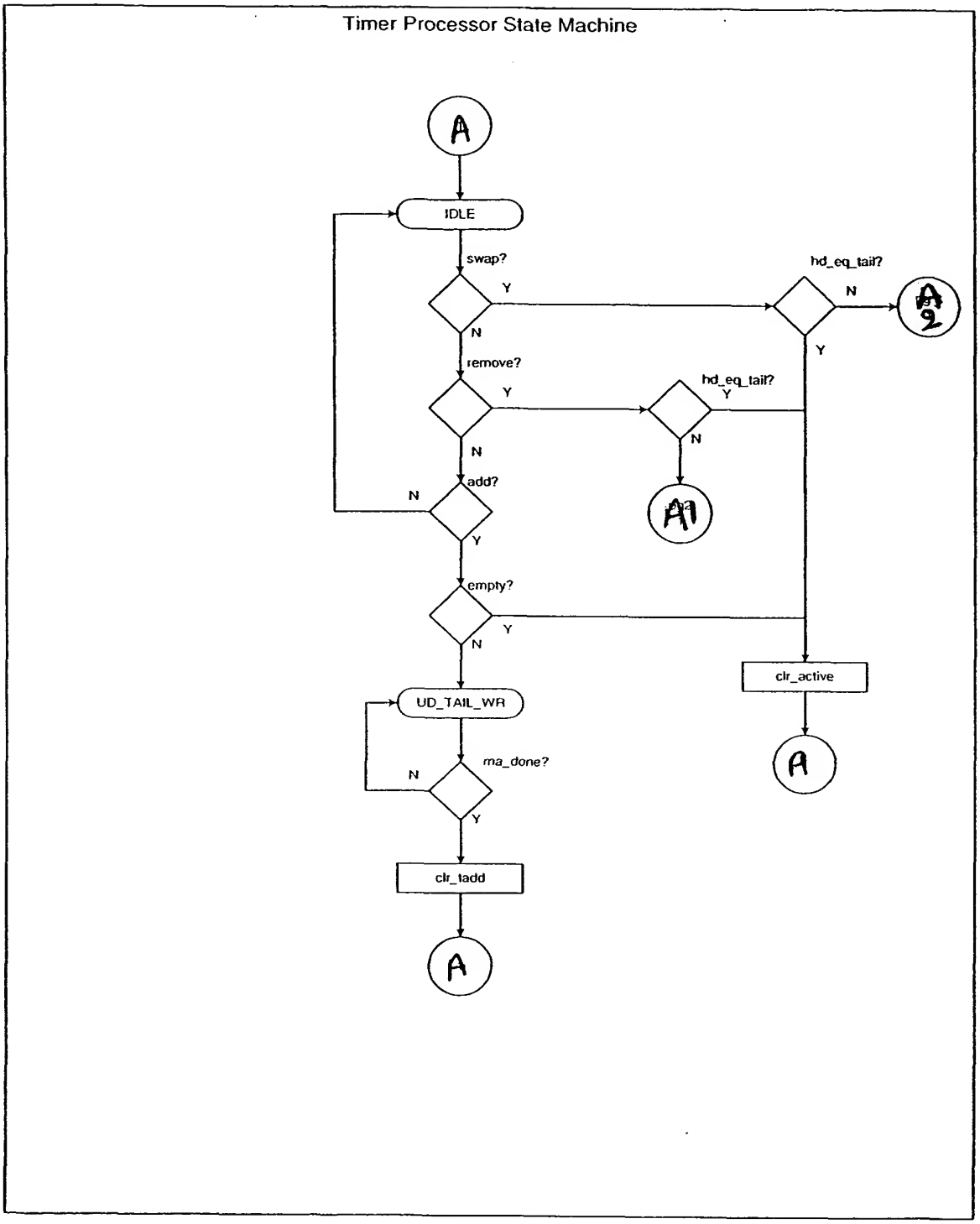
Timer Processor State Machine
A
IDLE
swap?
Y
N
hd_eq_tail?
N
Y
A2
remove?
Y
hd_eq_tail?
Y
N
N
add?
N
Y
A1
empty?
Y
N
clr_active
UD_TAIL_WR
ma_done?
N
Y
A
clr_tadd
A

Figure 3L9A

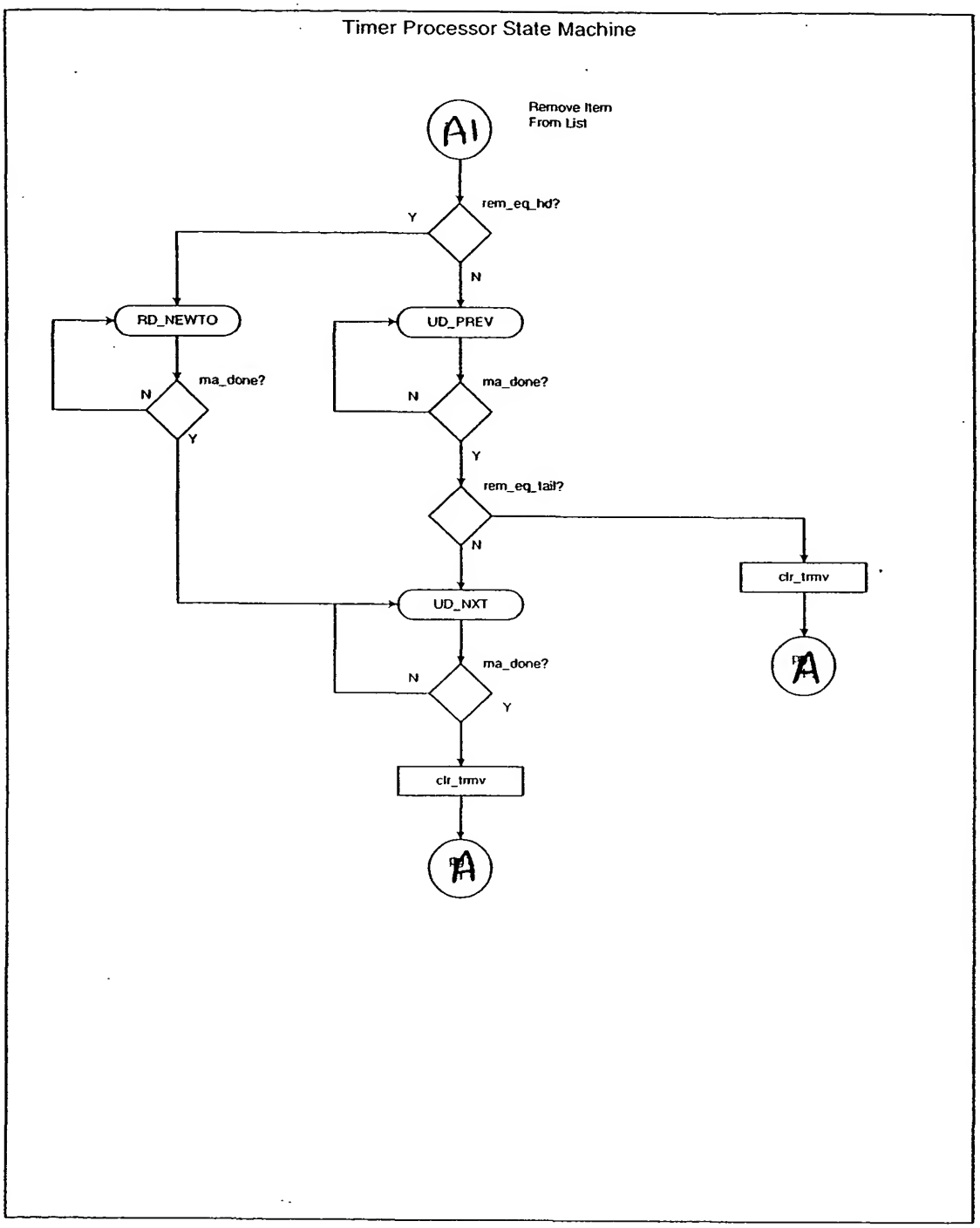
Timer Processor State Machine
A1
Remove Item
From List
rem_eq_hd?
Y
N
RD_NEWTO
UD_PREV
ma_done?
N
Y
ma_done?
N
Y
rem_eq_tail?
N
clr_trmv
UD_NXT
ma_done?
N
Y
clr_trmv
A
A

Figure 3L9B:

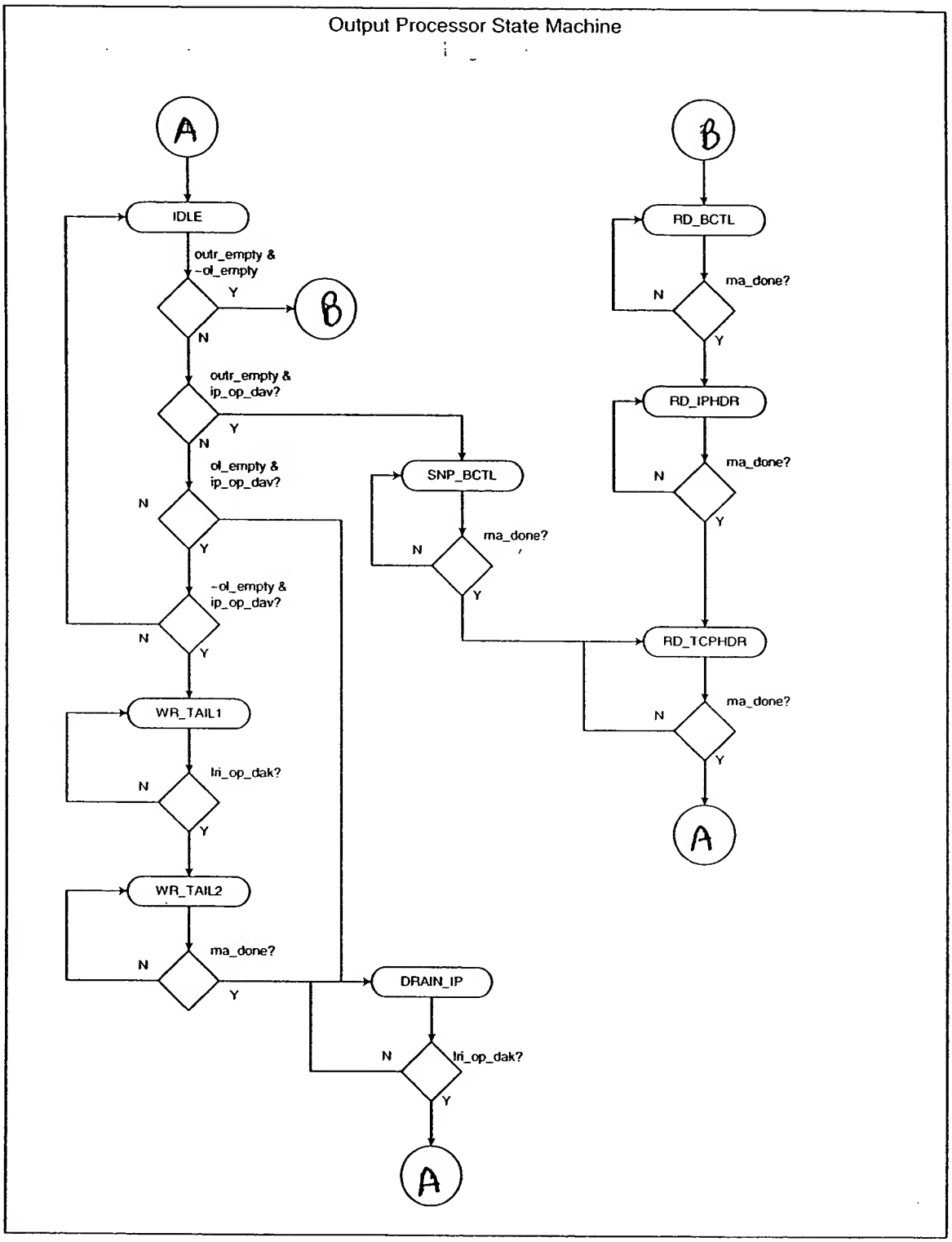
Output Processor State Machine
A
IDLE
outr_empty &
~ol_empty
Y
B
N
outr_empty &
ip_op_dav?
Y
N
ol_empty &
ip_op_dav?
N
Y
~ol_empty &
ip_op_dav?
N
Y
WR_TAIL1
N
Iri_op_dak?
Y
WR_TAIL2
N
ma_done?
Y
DRAIN_IP
N
Iri_op_dak?
Y
A
SNP_BCTL
N
ma_done?
Y
B
RD_BCTL
N
ma_done?
Y
RD_IPHDR
N
ma_done?
Y
RD_TCPHDR
N
ma_done?
Y
A

Figure 3L10 -

50 9-57

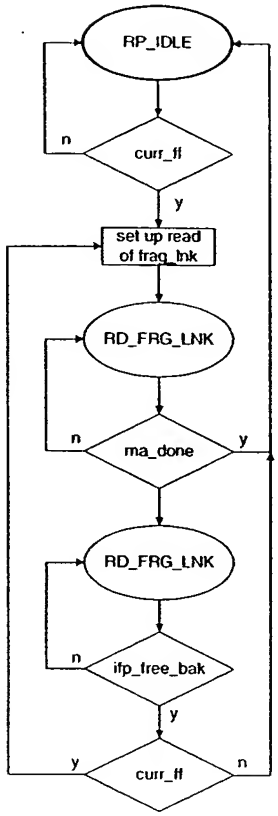

Figure 3L11 - Return Processor State Machine

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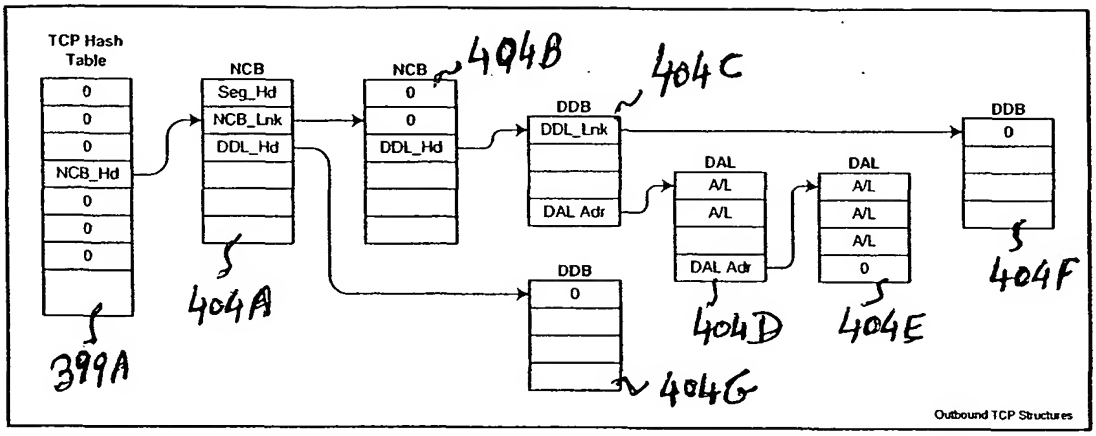

Figure 4A

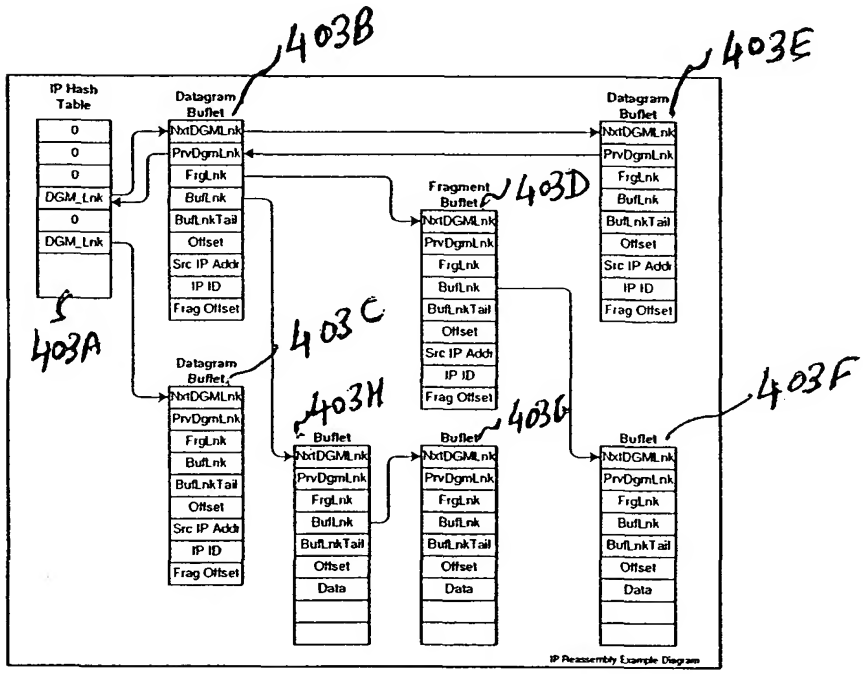

Figure 4B